APPLICATION NOTES

Testing Timing Over Packet With The Ixia Anue 3500

Testing according to ITU-T G.8261-2008 Appendix VI

26601 Agoura Road Calabasas, CA 91302 | Tel + 1-818-871-1800 | Fax + 1-818-871-1805 | www.ixiacom.com P/N: 915-6557-01 Rev. B June 2013

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Overview

In response to increased demand for advanced mobile broadband services, carriers and network providers are migrating their mobile backhaul networks from legacy synchronous transports such as SONET/SDH and T1/E1 to Carrier Ethernet. One technology to deliver synchronization services over these packet networks is IEEE 1588 (precision time protocol, PTP). The ITU-T G.8261 standard provides network limits and test cases to evaluate the performance of the synchronization services on these networks. Testing equipment according to this standard is key to marketing these synchronization devices for both network equipment manufacturers as well as service providers.

In a packet-based timing network, a master device produces packets either at a precise rate or with precisely recorded origin timestamps. These packets are added to the stream of background traffic that exists on the network. As a result of this mixing of traffic, each timing packet may experience a different amount of transmission delay. This effect is known as Packet Delay Variation, or PDV. This PDV affects the ability of the slave device to recover a physical clock accurately. The quality of clock recovery by the slave in the presence of this type of impairment must be measured.

The Ixia Anue G.8261 and MEF 18 test suites for the 3500 network emulator are specifically designed for evaluating the clock recovery performance of Circuit Emulation (CES) and Timing over Packet (ToP) solutions under a variety of real-world network conditions. The G.8261 test suite covers all seventeen test cases and their various iterations as defined in ITU-T G.8261 (2008) Appendix VI. The MEF 18 test suite covers the eight test cases found within section 6 “Synchronization” of the MEF 18 test plan, which call for the creation of Packet Delay Variation (PDV) scenarios. ToP technology (including CES) is very sensitive to the PDV and loss conditions found in packet switched networks. Therefore it is critical to verify the performance of the clock recovery algorithms found within these devices against real-world PDV and loss conditions prior to deployment.

ITU-T G.8261 Appendix VI suggests one way to accomplish this is to build a mock network in the lab. However, these mock networks have many shortcomings, which are overcome by utilizing network emulation technology to create the PDV and loss conditions required for testing. Emulation is far more accurate, repeatable and flexible compared with building a mock network.

The Ixia Anue G.8261 and MEF 18 test suites precisely recreate the PDV and loss conditions produced for each ‘network scenario’ (number of switches and disturbance load characteristics) described within each ITU-T G.8261 (2008) and MEF 18 test case.

ITU-T G.8261

ITU-T G.8261 specifies network wander limits for ToP (e.g., IEEE 1588) or CES across an NGN packet based network. G.8261 (2008) describes seventeen test cases within Appendix VI as a guideline to the industry for evaluating the clock recovery performance of both CES and ToP solutions. See Table 1 below for a list of test cases. Metrics such as TIE, MTIE, and frequency accuracy are measured during testing for validation against G.823, G.824 and G.8261 requirements. Figure 2 below shows the mock network described within G.8261 Appendix VI which includes 10 Ethernet switches connected in series with disturbance load traffic generators. With the Ixia Anue 3500, network emulation replaces the 10 Ethernet switches and disturbance load traffic generators, and the timing measurements are made in real time during the test.

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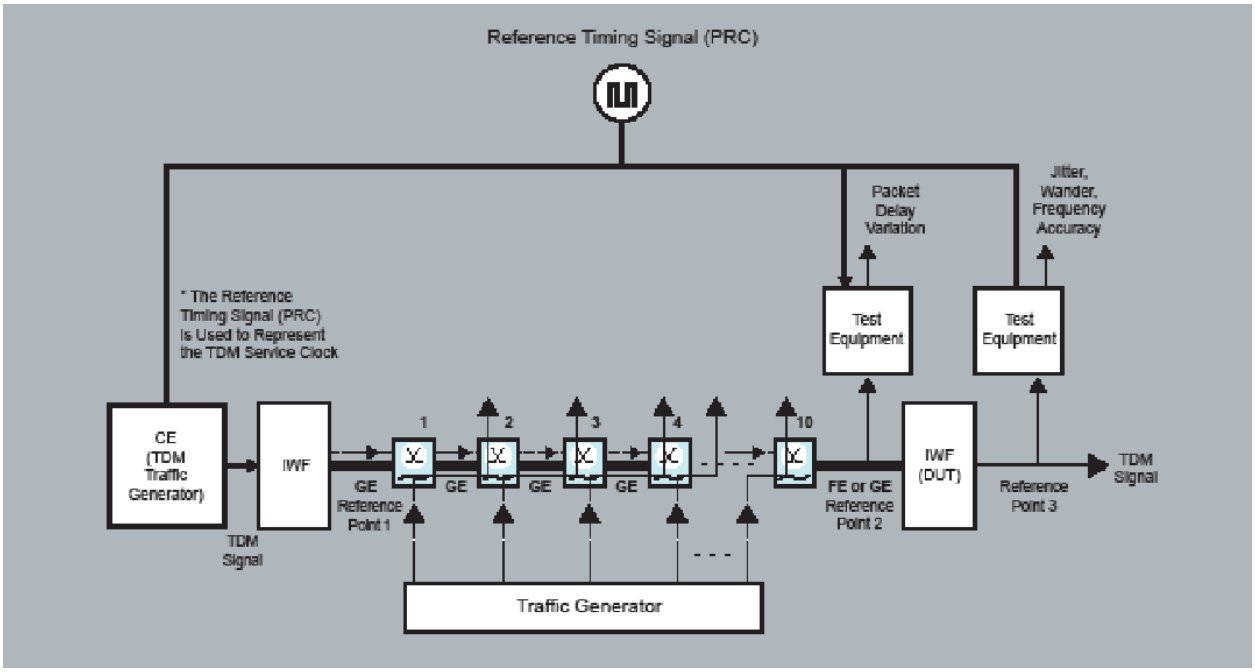

Figure 1: ITU-T G.8261 Test Diagram – 10 Switches in a Mock Network

By using an Ixia Anue 3500 Network Emulator in place of the Ethernet switches as defined in the G.8261 Appendix VI Test Topology diagrams, it is possible to test against more realistic delay variation profiles and also create a highly repeatable test methodology.

MEF 18

Metro Ethernet Forum's MEF 18 defines abstract test procedures to verify that TDM services such as DS1, E1, DS3 and E3 transported over CES can be delivered with the required minimum output jitter and wander. MEF 18 certification testing is conducted by an officially endorsed test lab, and that lab uses network emulators running the Ixia Anue MEF 18 test suite. It is therefore advantageous for companies to pre-test their systems with the same test set up prior to formal MEF 18 certification testing. Table 1 contains a list of the test cases.

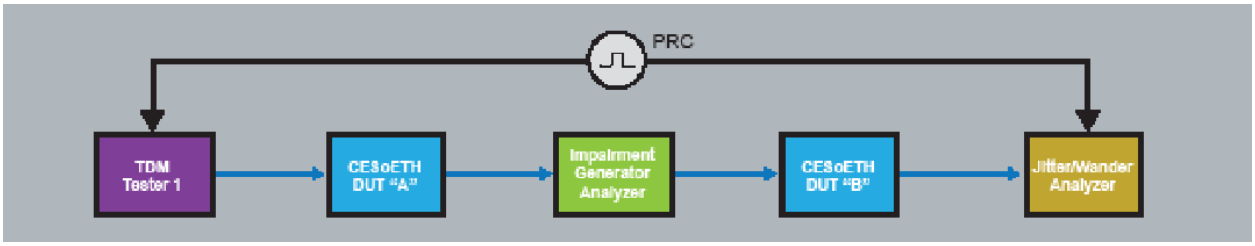

Figure 2: MEF 18 Test Bed as Shown in MEF 18 Test Plan

Description	MEF 18 "Test Case 6 - Synchronization"	ITU-T G.8261 Appendix VI April 2008
Static Packet Load	NA	Test Case 1 (VI.3.2.2)
Sudden large network load changes - 80% to 20%	6.1 Only Traffic Model 2 (TM2)	Test Case 2 (VI.3.2.3)
Slow long timescale changes in network load - 1% steps, 20% to 80%	6.2 Only TM2	Test Case 3 (VI.3.2.4)
Temporary network outages (10s shorter outage)	6.3 10 sec outage and TM2	Test Case 4 (VI.3.2.5)
Temporary network outages (100s longer outage)	Temporary network outages (100s longer outage)	
6.4 100 sec outage and TM2	6.4 100 sec outage and TM2	
Test Case 4 (VI.3.2.5)	Test Case 4 (VI.3.2.5)	
Temporary 100% network congestion (10s shorter disturbance)	Temporary 100% network congestion (10s shorter disturbance)	
6.5 10 sec disturbance and TM2	6.5 10 sec disturbance and TM2	
Test Case 5 (VI.3.2.6)	Test Case 5 (VI.3.2.6)	
Temporary 100% network congestion (100s longer disturbance)	Temporary 100% network congestion (100s longer disturbance)	
Route changes caused by network failure (small change)	Route changes caused by network failure (small change)	
6.7 Bypass 1 switch and TM2	6.7 Bypass 1 switch and TM2	

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Description	MEF 18 "Test Case 6 - Synchronization"	ITU-T G.8261 Appendix VI April 2008
Test Case 6 (VI.3.2.7)	Test Case 6 (VI.3.2.7)	
Route changes caused by network failure, 40% load	Route changes caused by network failure, 40% load	
6.8 Bypass 5 switches and TM2	6.8 Bypass 5 switches and TM2	
Differential clock recovery method with noise added	NA	Test Case 10 (VI.4.2)
Differential clock recovery method with temporary network congestion	NA	Test Case 11 (VI.4.3)
Network disturbance load with 80% forward direction, 20% reverse	NA	Test Case 12 (VI.5.2.2)
Sudden large and persistent changes in network load	NA	Test Case 13 (VI.5.2.3)
Slow change in network load over an extremely long timescale	NA	Test Case 14 (VI.5.2.4)
Test temporary network outages and restoration	NA	Test Case 15 (VI.5.2.5)
Test temporary network congestion and restoration	NA	Test Case 16 (VI.5.2.6)
Route changes caused by network failure, 40% forward load and 30% reverse	NA	Test Case 17 (VI.5.2.7)

Table 1: Comparison of G.8261 (2008) and MEF 18 Test Cases

Details of these requirements are available in the following standards:

- Recommendation ITU-T G.8261 – Timing and synchronization aspects in packet networks
- MEF 18 - Abstract Test Suite for Circuit Emulation Services over Ethernet based on MEF 8

Acronyms and Definitions

1PPS	One Pulse Per Second
CES	Circuit Emulation Service
DUT	Device Under Test
EEC	Ethernet Equipment Clock
GMC	Grand Master Clock
IWF	Inter-Working Function
MEF	Metro Ethernet Forum
MTIE	Maximum Time Interval Error
NGN	Next Generation Network
OC	Ordinary Clock
PDH	Plesiochronous Digital Hierarchy
PDV	Packet Delay Variation
PEC	Packet Equipment Clock
Phase noise	See Wander
PRC	Primary Reference Clock
PTP	Precision Time Protocol (IEEE1588v2)
SEC	SONET/SDH Equipment Clock
SyncE	Synchronous Ethernet
TDEV	Time Deviation
TDM	Time Division Multiplex
TIE	Time Interval Error
ToD	Time of Day
ToP	Timing over Packet
Wander	Phase variation of the clock signal with respect to an ideal reference clock at a rate less than 10 Hz

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Test Bed Topology

G.8261 testing is accomplished primarily by measuring wander (low frequency phase variation) on the recovered clock interface of the slave or Ordinary Clock (DUT), while the specified packet impairment is applied in-line between the Grand Master Clock and the Ordinary Clock. The Ixia Anue 3500 and the Grand Master Clock are provided with a common reference clock; normally this is a clock signal sent to the 3500 from the Grand Master Clock over 2.048MHz BNC, 10MHz BNC, T1 BITS RJ48C, or E1 MTS RJ48C.

Required Equipment and Software

- Ixia Anue 3500
- Host PC
- Grand Master Clock – with reference clock output
- DUT – Ordinary Clock / Slave Clock to be tested

Test System Diagram

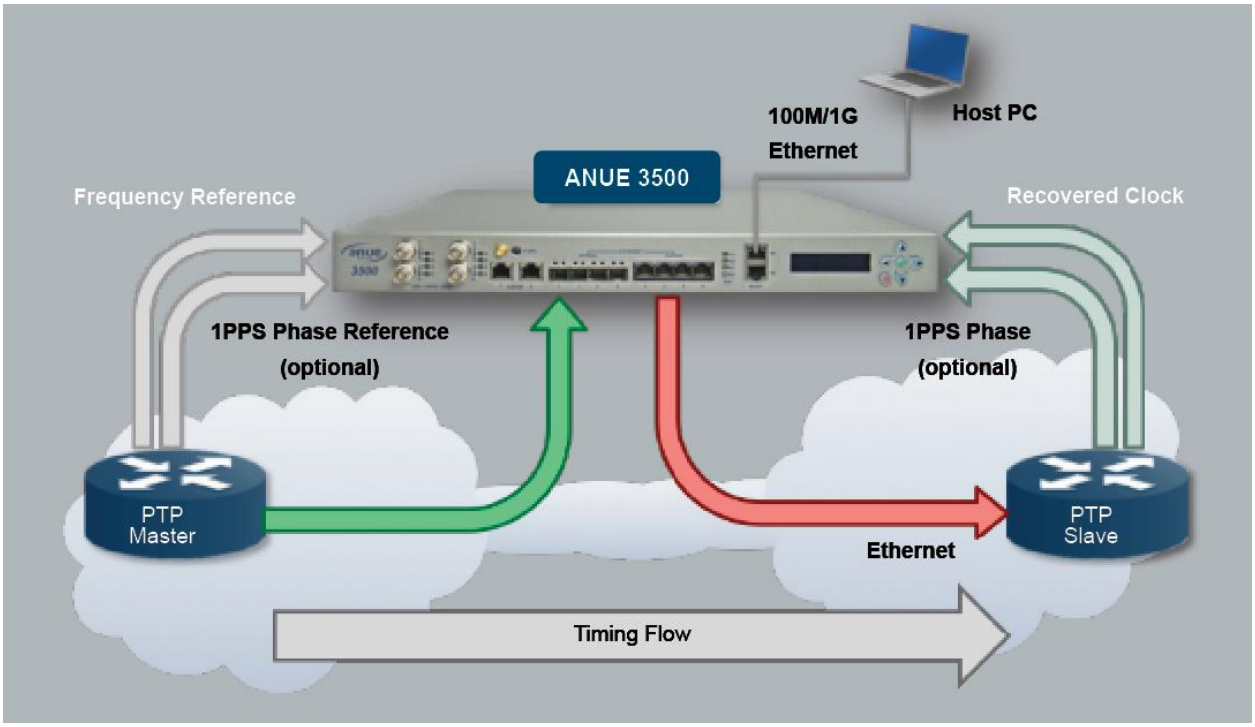

Figure 3: Test Topology Diagram

Test System Setup

1) In this setup, the 3500 is connected to an external frequency reference. This external frequency reference must be synchronized with the Grand Master. Many Grand Master Clocks have frequency outputs that can be used for this purpose, or alternately the Grand Master Clock and the 3500 may both derive their reference from the same source. The flexibility of the Ixia Anue 3500 allows numerous options for providing a timing reference to the 3500.

Reference	Connection	Details
Internal GPS	SMA Antenna front panel	Frequency, Phase & Time of Day Reference
External GPS	BNC or PDH Frequency, BNC 1PPS RS-232/422 ToD	Frequency, Phase & Time of Day Reference
External Phase	BNC or PDH Frequency, BNC 1PPS	Frequency & Phase Reference
External Frequency	BNC or PDH	Frequency Reference
Internal OXCO		Stratum 3 internal reference; optionally use with external phase signal
Internal Rubidium		Optional; Stratum 2 capable; Use with internal GPS for disciplined reference

Table 2: Connecting Clock Input Interface to the Ixia Anue 3500

Note: The internal rubidium oscillator is an optional feature that is factory installed onto the Time of Day Interface Module.

A frequency reference is required, at a minimum, for G.8261 testing. Phase and Time of Day references are optional for frequency tests.

For 1588 Time Error measurements, both Time of Day and Phase references are required. Please see the Ixia Anue 3500 User Guide for information on input reference signals.

G.8261 Testing

ITU-T G.8261 describes 17 test cases, the purpose of which is to evaluate the ability of the DUT to recover frequency accurately and provide synchronization, in the presence of impairment resulting from traffic on the network between the master clock and the DUT.

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These test cases follow a common procedure. The differences between each of the test cases are related to the choice of impairments being applied between the master and slave clocks. In general, this testing can be described as follows:

- Connect the Ixia Anue 3500 in-line between the master clock and the DUT (slave clock) using Ethernet
- Connect the recovered clock interface from the slave clock (DUT) to the Ixia Anue 3500 for measurement
- Once synchronization has been achieved between the master and slave clocks, begin Network Playback of the appropriate impairment AIT file from the G.8261 Test Suite
- Measure the following according to G.8261 Appendix VI:
  - TIE, MTIE, TDEV (record the TIE of the recovered clock)
  - Frequency accuracy
  - Packet Delay Variation (PDV)
  - Verify the performance meets the applicable limits

All test cases utilize the test bed topology described above, or a variant of the described test topology.

The 17 different test cases each require impairment profiles, which are used by the Ixia Anue 3500 to emulate the impairment described by each test case. These impairment files (AIT files) are provided on the **G.8261 Test Suite DVD.**

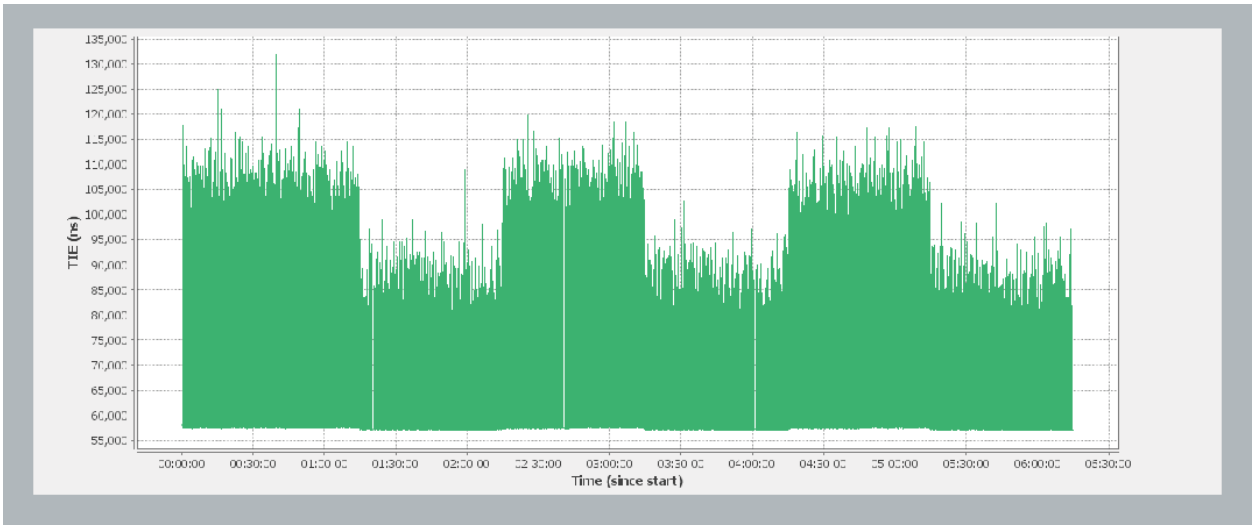

Figure 4: Example PDV Profile from the Ixia Anue G.8261 Test Suite

The G.8261 test cases are a superset of the MEF 18 test cases.

The G.8261 test cases are applicable to Timing over Packet networks using Precision Time Protocol (PTP / IEEE1588) or networks using Circuit Emulation Services (CES, such as SAToP or CESoP).

G.8261 Test Cases 1-17 with PTP / IEEE1588

Timing over Packet networks may utilize Precision Time Protocol (PTP) which is defined by IEEE1588. PTP is an adaptive clock recovery technology in which packets containing precise time stamps are sent at a specified rate by the Grand Master Clock across a packet network. These packets are received by a slave device such as an Ordinary Clock or Boundary Clock, and then through a two-way time transfer, the slave device recovers a clock synchronous with that of the Grand Master Clock. This recovered clock is provided on a physical interface in one of a number of formats including T1, E1, 2.048 MHz and 10 MHz. The testing is accomplished by measuring the recovered clock on the slave DUT while the specified impairment is being introduced between the Grand Master and the DUT.

For additional details see ITU-T G.8261, Appendix VI *Measurement guidelines for packet-based methods.*

Test Setup

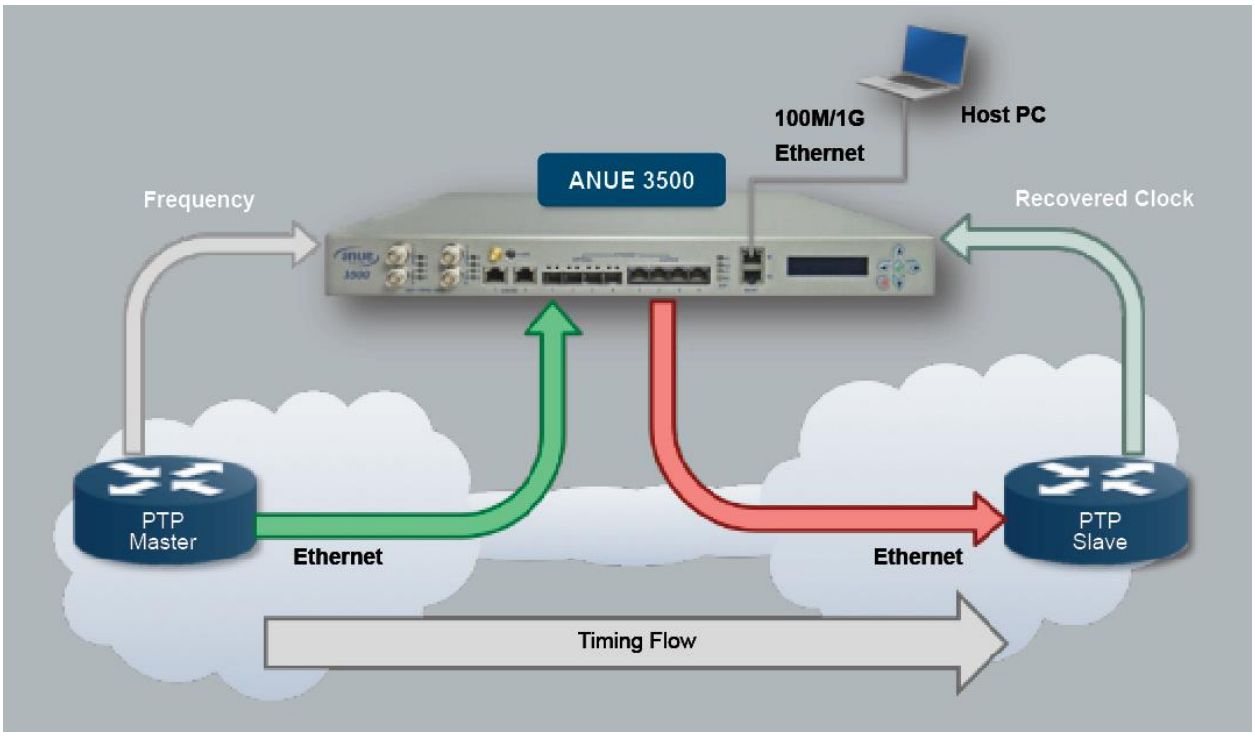

Figure 5 G.8261 Test Setup

1) Ensure the Ixia Anue 3500 and the Grand Master Clock are connected to a common frequency reference.
2) Configure a port-pair on the Ixia Anue 3500 for “Inline” mode, and if using 1G dual-media ports, configure for the correct media type and speed (copper or fiber, 100M or 1G) using the Ixia Anue 3500 Control Panel Ports tab. Double-click the port that will be connected to the Grand Master Clock’s Ethernet port. This will bring up the Ethernet Port Property dialog.

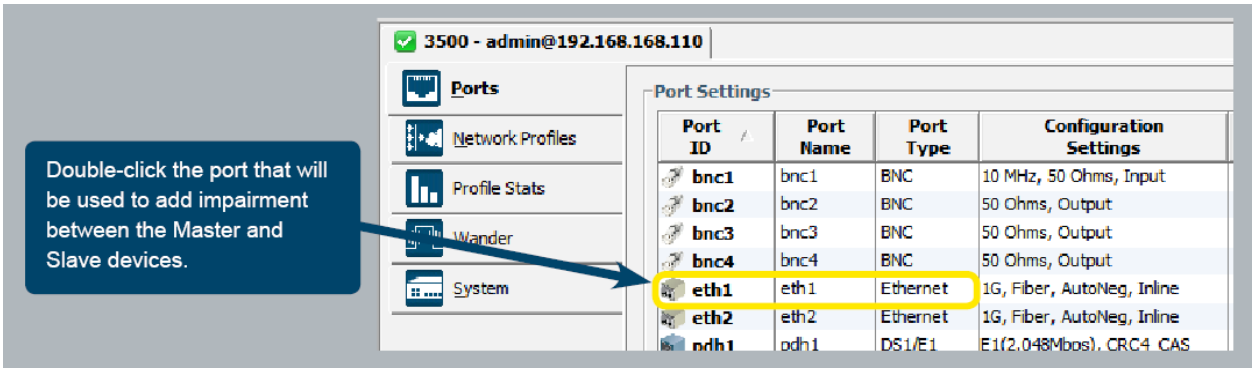

Figure 6: Selecting the Ethernet Port Connected to the DUT

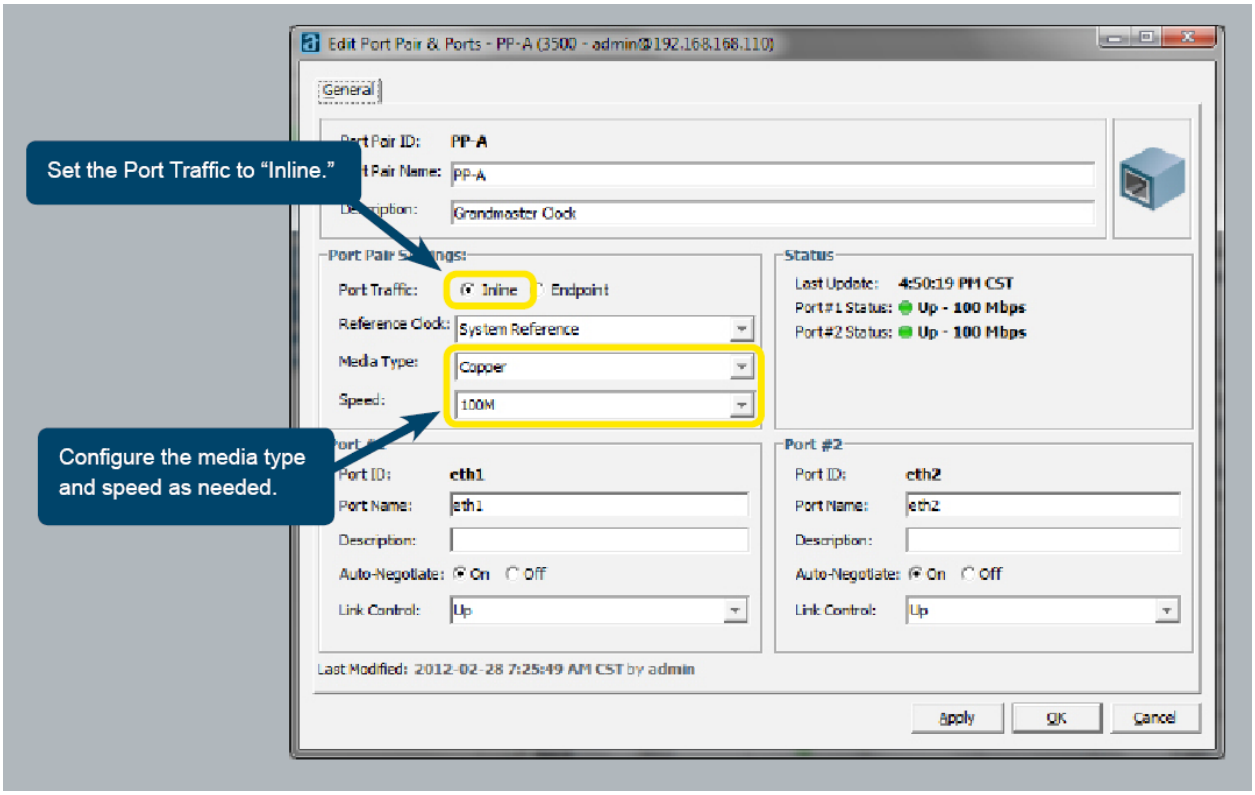

Figure 7: Configuring the Ethernet Port Pair

3) Connect the Grand Master Clock's Ethernet port to Eth1 and connect the Slave (DUT) Ethernet port to Eth2 (use Xeth1 and Xeth2 for 10G). Be sure to note which port is connected to the Grand Master and which is connected to the Slave. This information will be required in order to correctly configure the Network Profiles.

4) Connect the Slave DUT's recovered clock interface to the Ixia Anue 3500 using the appropriate interface (BNC, PDH or Ethernet). Configure the Ixia Anue 3500 interface to match the frequency and framing of the Slave DUT's interface that is to be measured.

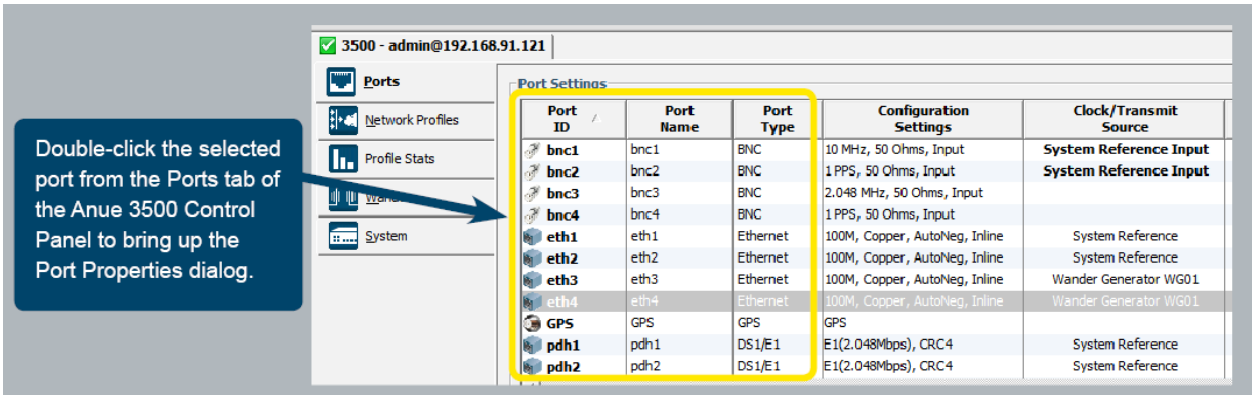

Figure 8: Selecting the Recovered Clock Measurement Port

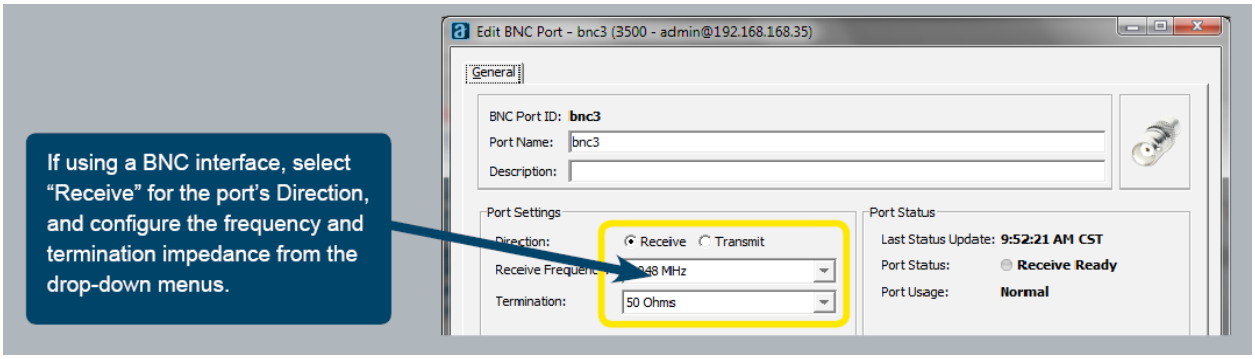

Figure 9: Configuring a BNC Interface

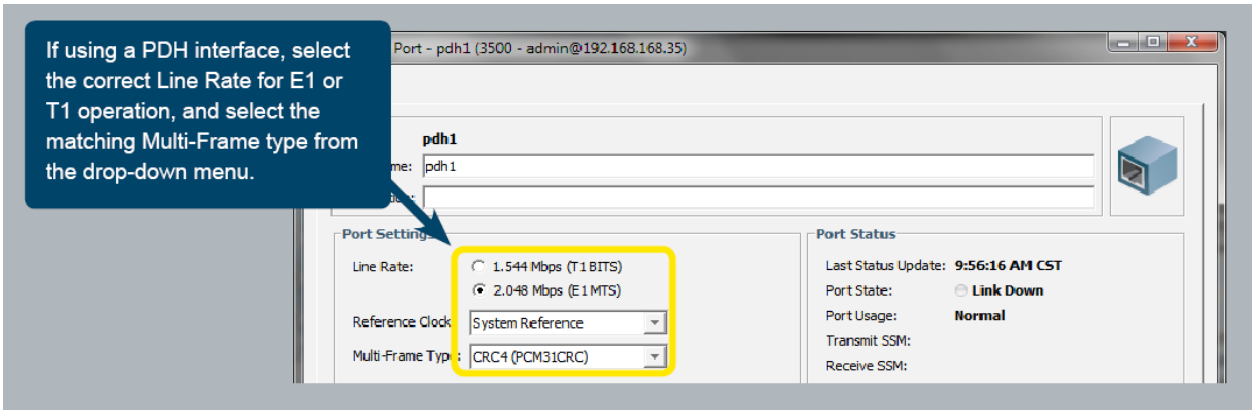

Figure 10: Configuring a PDH Interface

5) Select a Wander Measurer from the Ixia Anue 3500 Control Panel's Wander tab to measure the recovered clock interface. Configure the Wander Measurer for the correct interface.

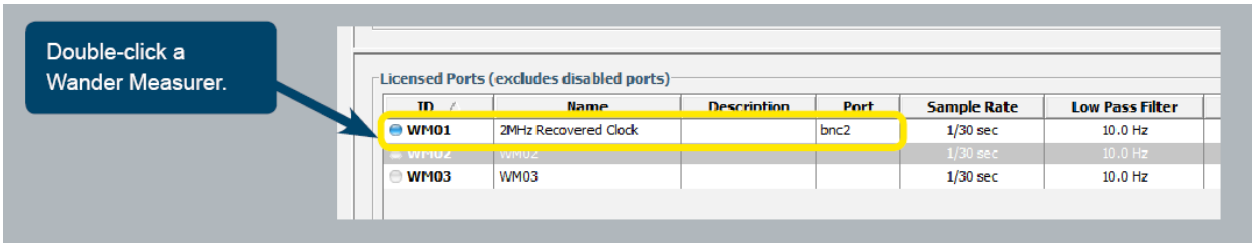

Figure 11: Selecting a Wander Measurer from the Wander tab

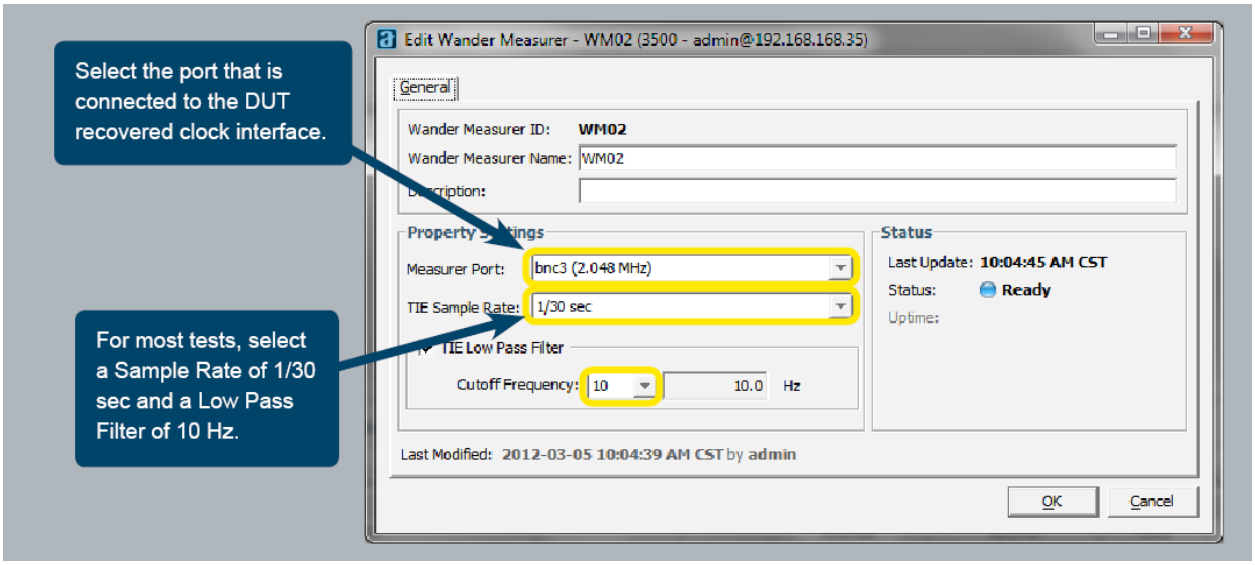

Figure 12: Editing the Wander Measurer

6) 6) Configure Network Profiles for each port used in the test (eth1 and eth2) using the Quick PTP option. Configure the Quick PTP settings to match your PTP packets.

Note: You must perform this procedure for both the port connected to the DUT and the port connected to the Grand Master Clock.

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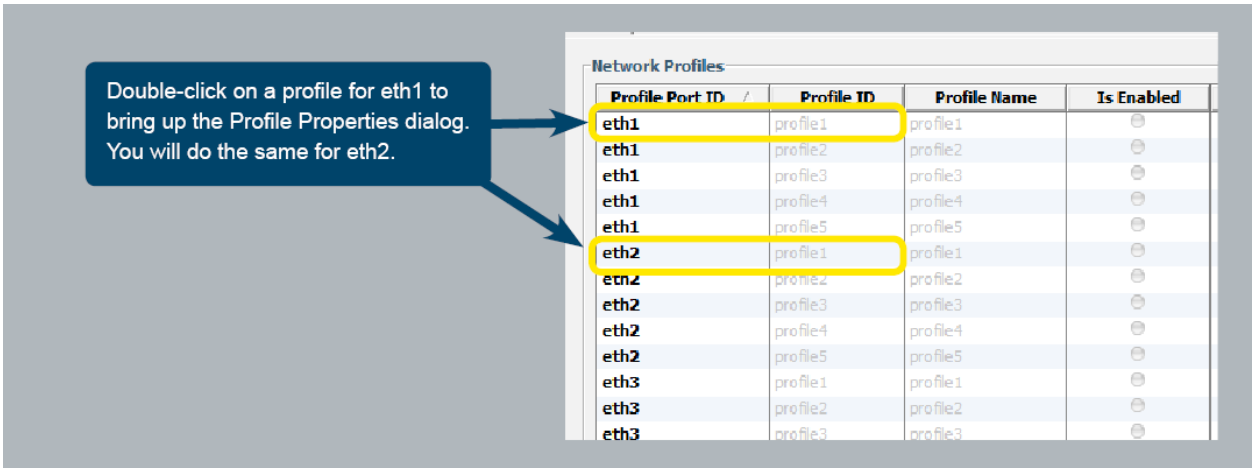

Figure 13: Selecting the Network Profile

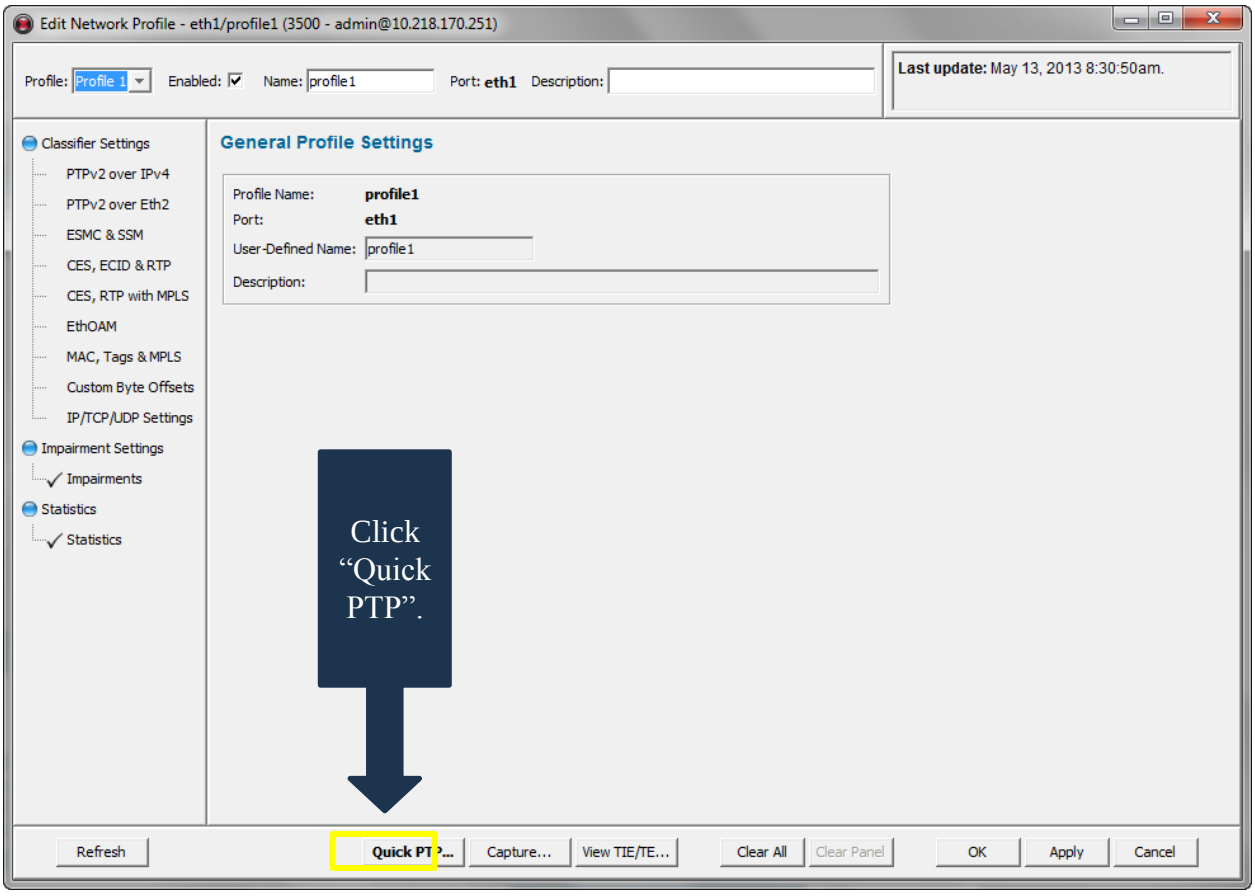

Figure 14: Enable a Network Profile and Open the Quick PTP Dialog

Select the appropriate PTP Packet Structure option and then configure the Master and Slave addresses. Click "OK"

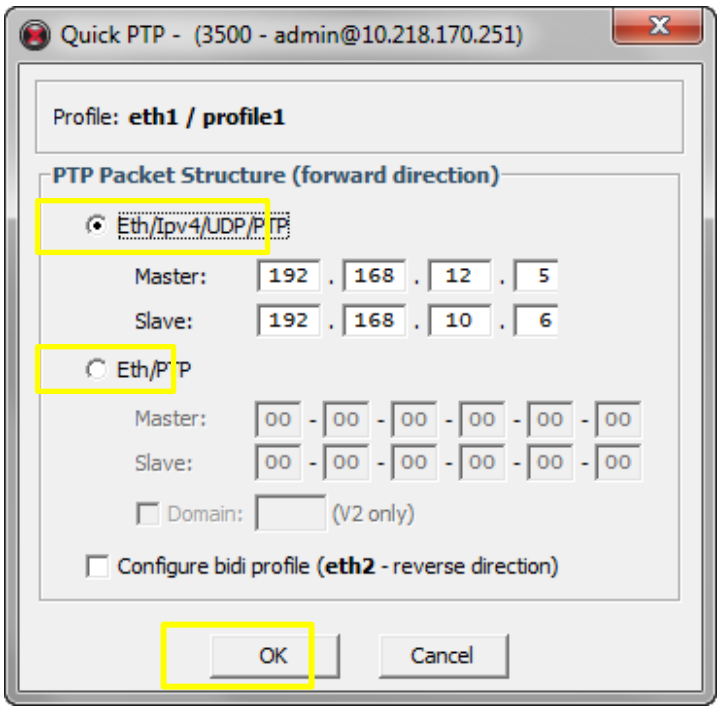

Figure 15: Configure the Quick PTP Dialog

7) Load the impairments for the test case that is to be run.

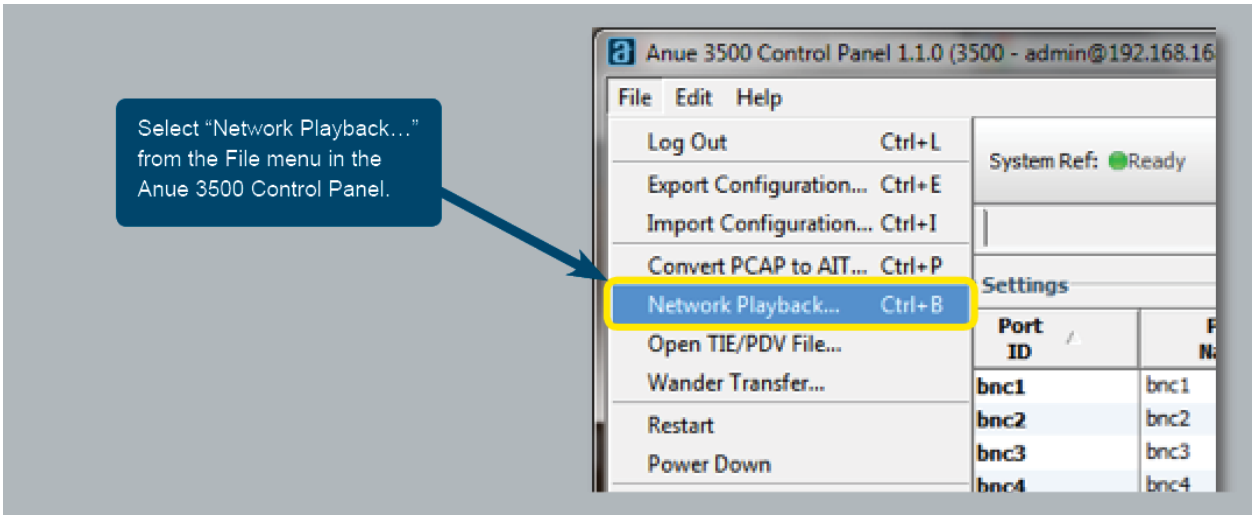

Figure 16: Network Playback

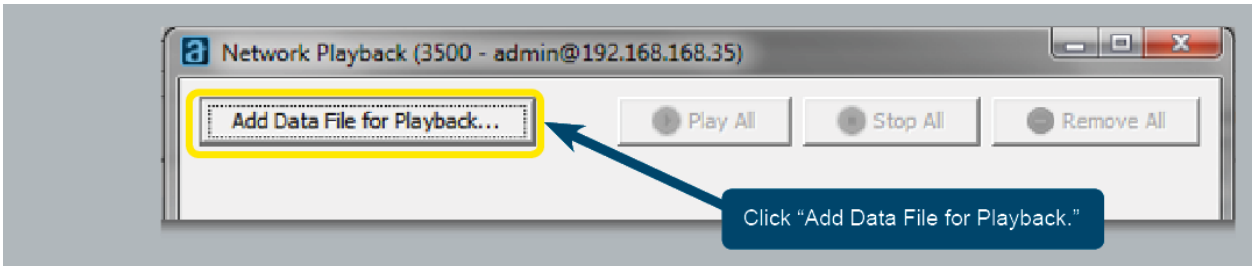

Figure 17: Adding Data File for Playback

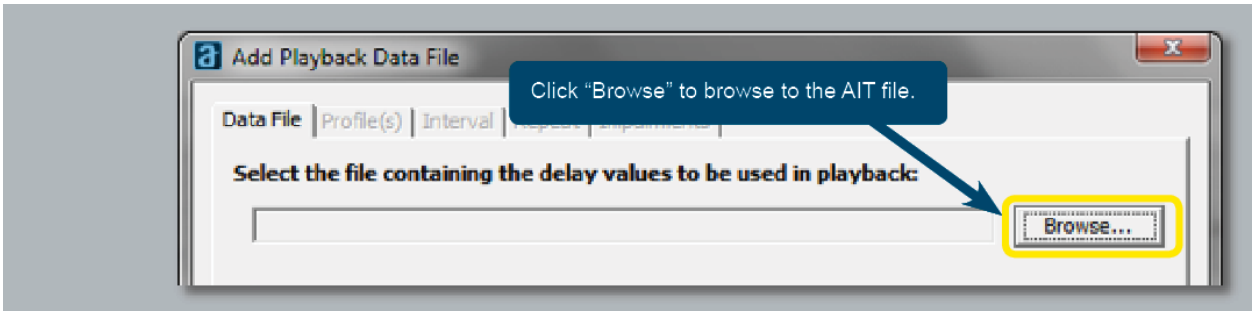

Figure 18: Click Browse

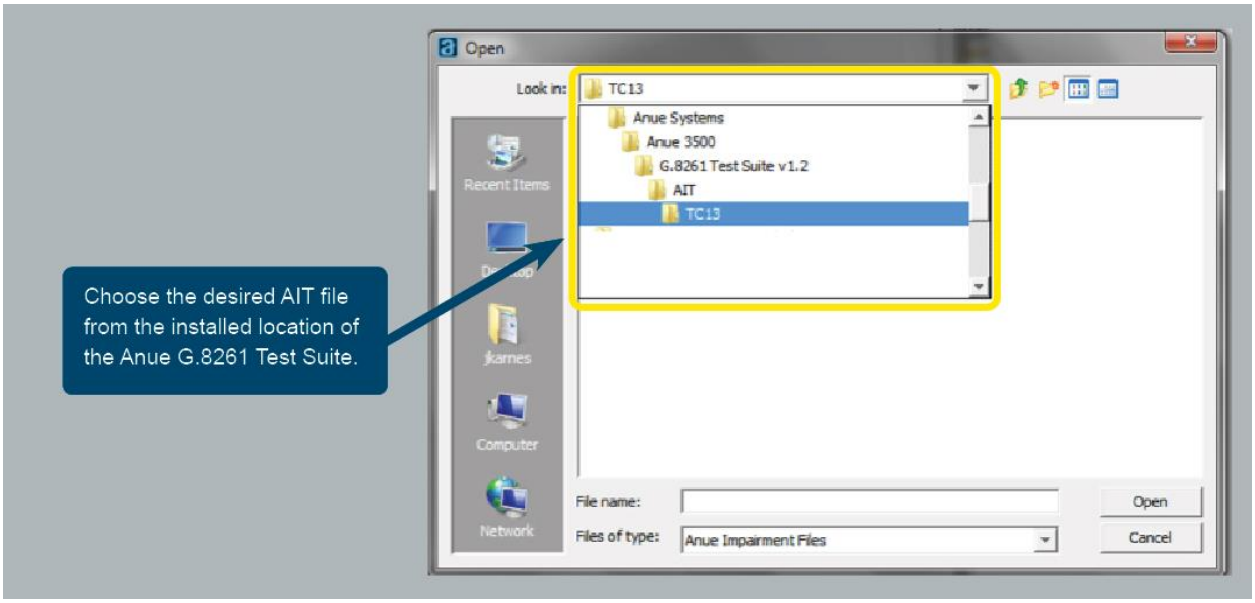

Figure 19: Browse to AIT file

Note: The Ixia Anue G.8261 Test Suite must be installed on the computer prior to running these impairments. The files are normally installed in the user directory such as "C:\users\username\Anue

Systems\Anue 3500\G.8261 Test Suite v1.2\AIT\TCnn" where "TCnn" refers to the test case. They are organized by number. For example, for Test Case 17, load "TC17".

For bidirectional tests, there will be a "_fwd" and a "_rev" file. Use the "_fwd" file on the profile for the port connected to the DUT slave device and use the "_rev" file on the profile for the port connected to the Grand Master Clock.

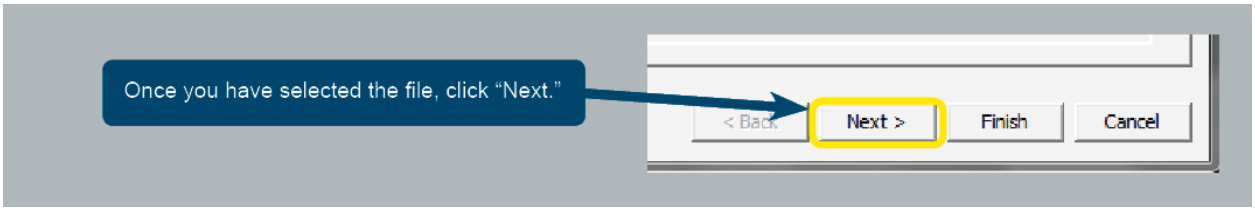

Figure 20: Click Next

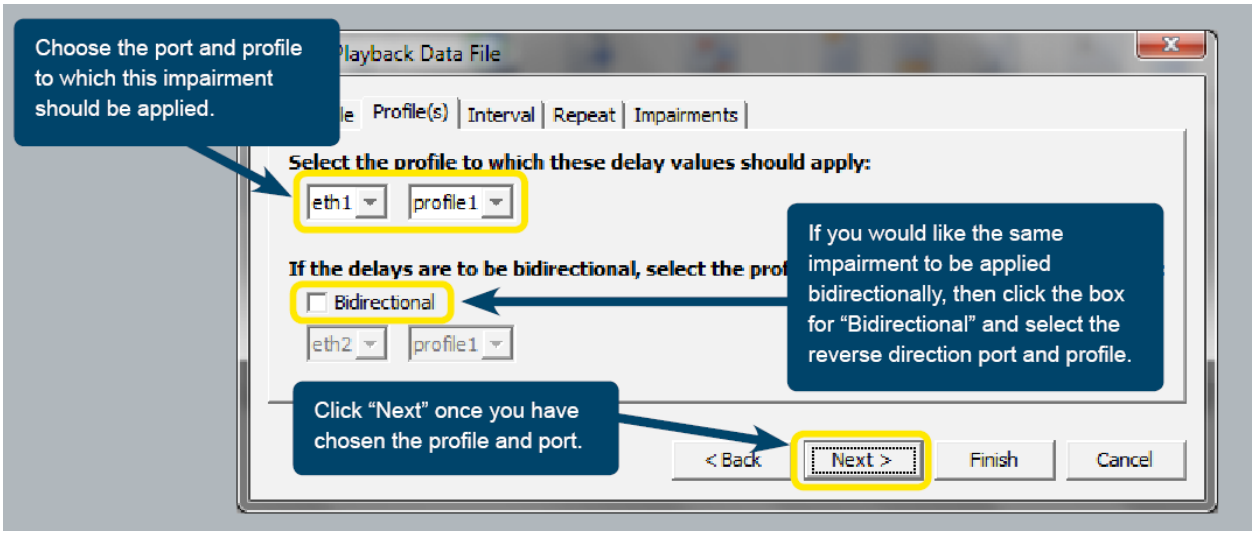

Figure 21: Configuring Network Playback

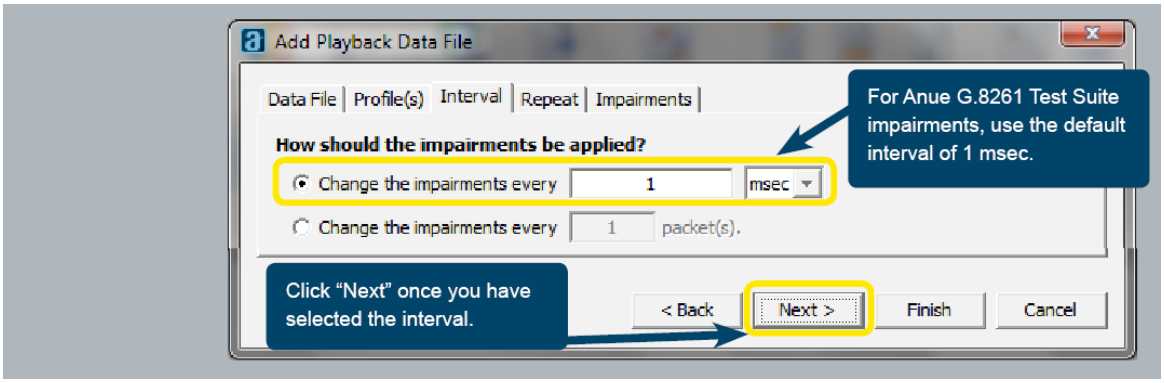

Figure 22: Configuring Network Playback

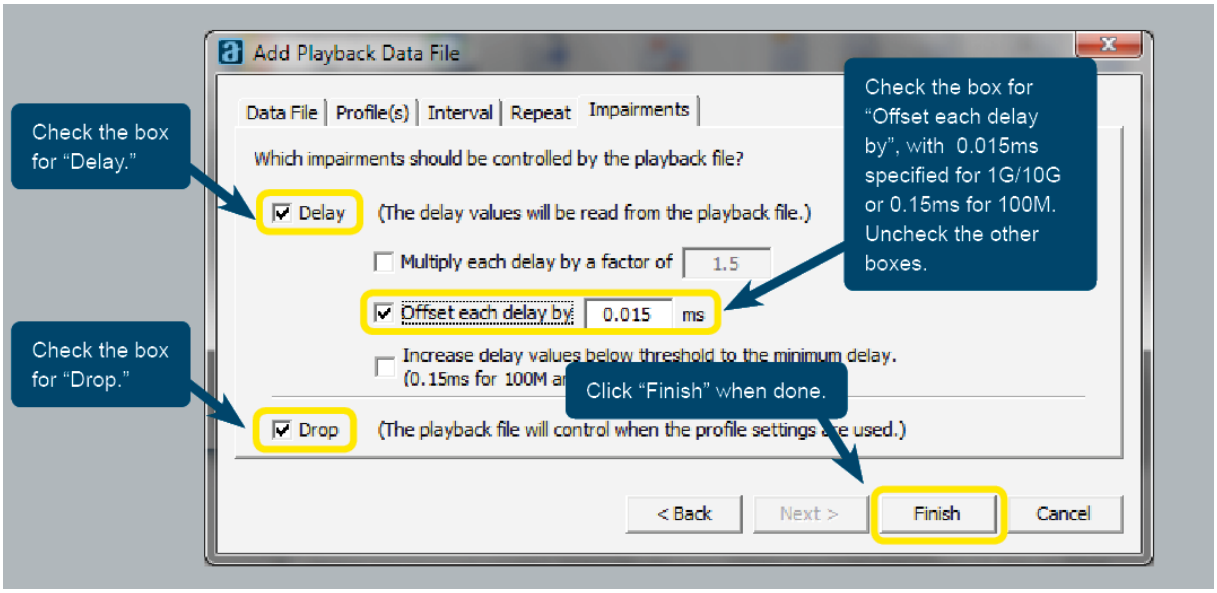

Figure 23: Configuring Network Playback

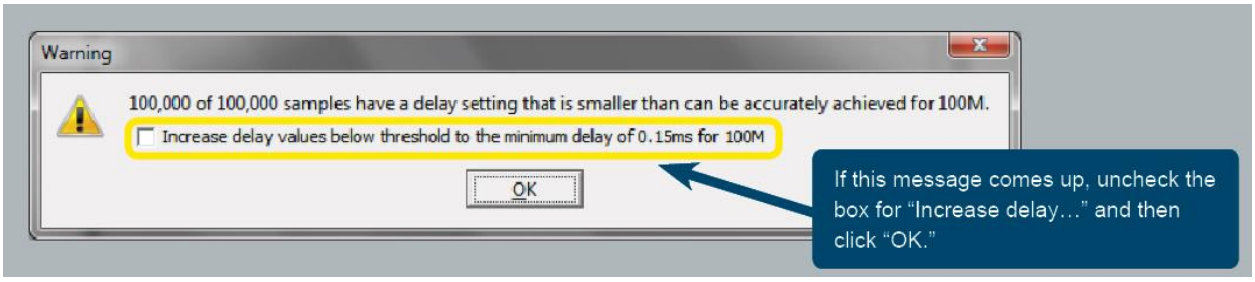

Figure 24: Clearing the "Increase Delay" Checkbox

This completes the Network Playback configuration. Note that you will actually begin playback of the AIT file in a future step.

8) The PTP Slave DUT may take up to an hour or longer to become synchronized with the Grand Master Clock. You can identify synchronization by monitoring the DUT's recovered clock TIE graph, and also by monitoring the user interface for indication of synchronization.

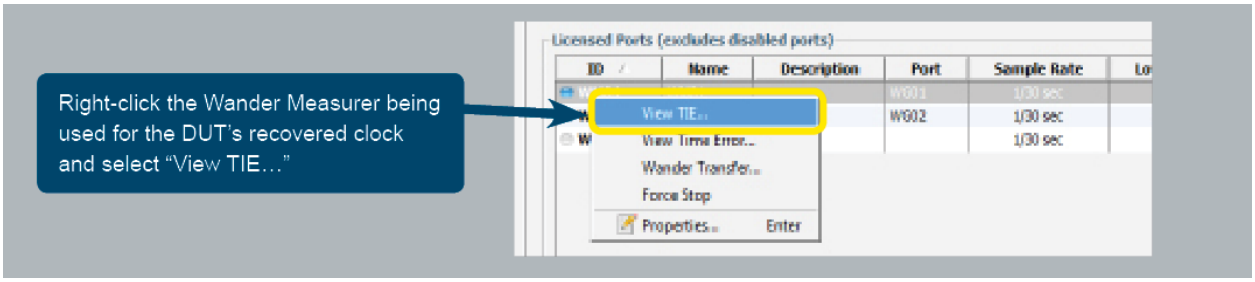

Figure 25: Selecting "View TIE..." for the Wander Measurer

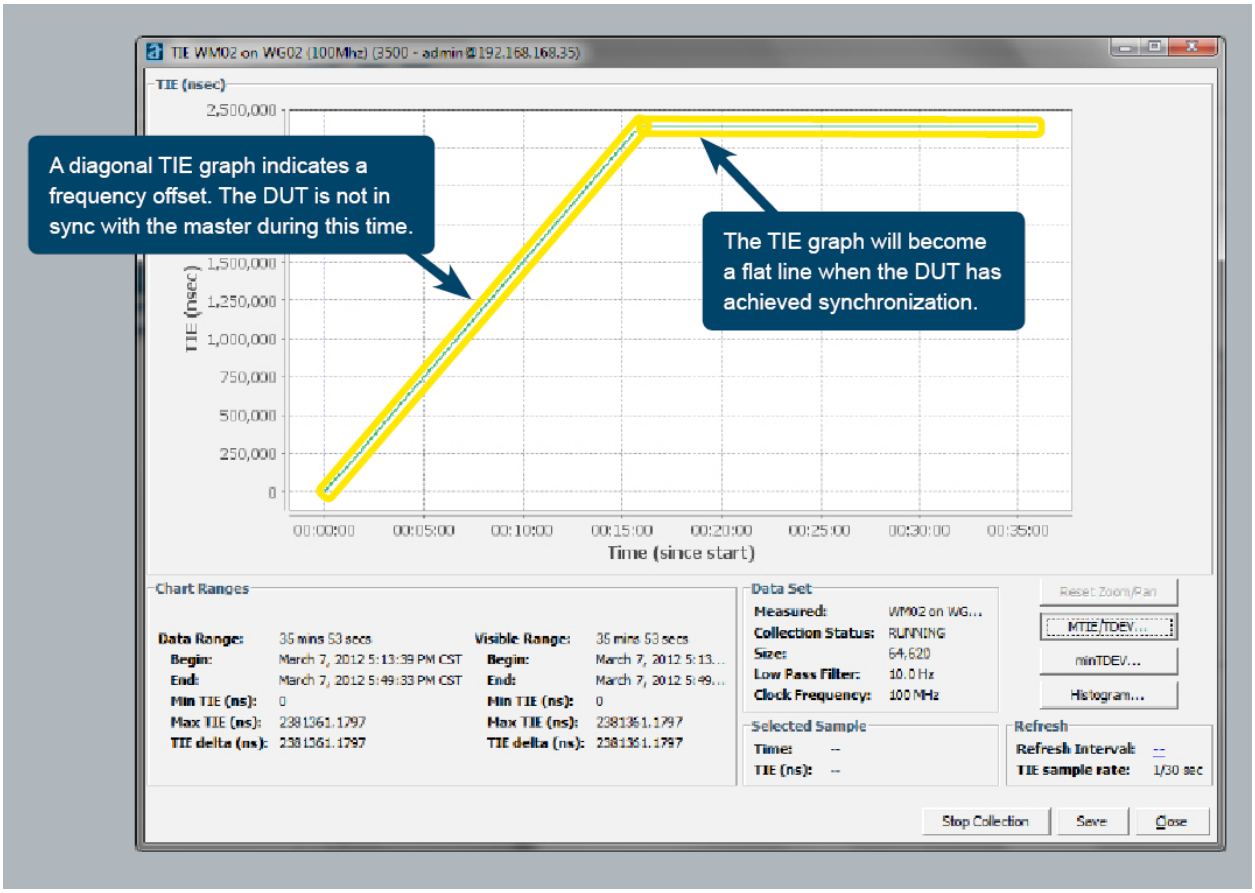

Figure 26: Monitoring TIE during Synchronization Phase

9) Once the DUT is in sync with the Grand Master, close the TIE window and restart the TIE measurement.

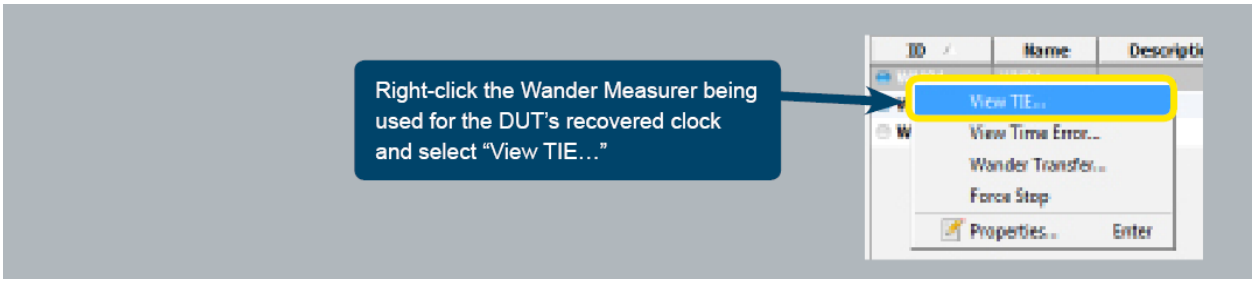

Figure 27: Starting the TIE Measurement

Test Steps

1) View the MTIE and TDEV results, including the Pass/Fail results against the masks that are applicable to your interface type by clicking the "MTIE/TDEV" button in the TIE graphical window.

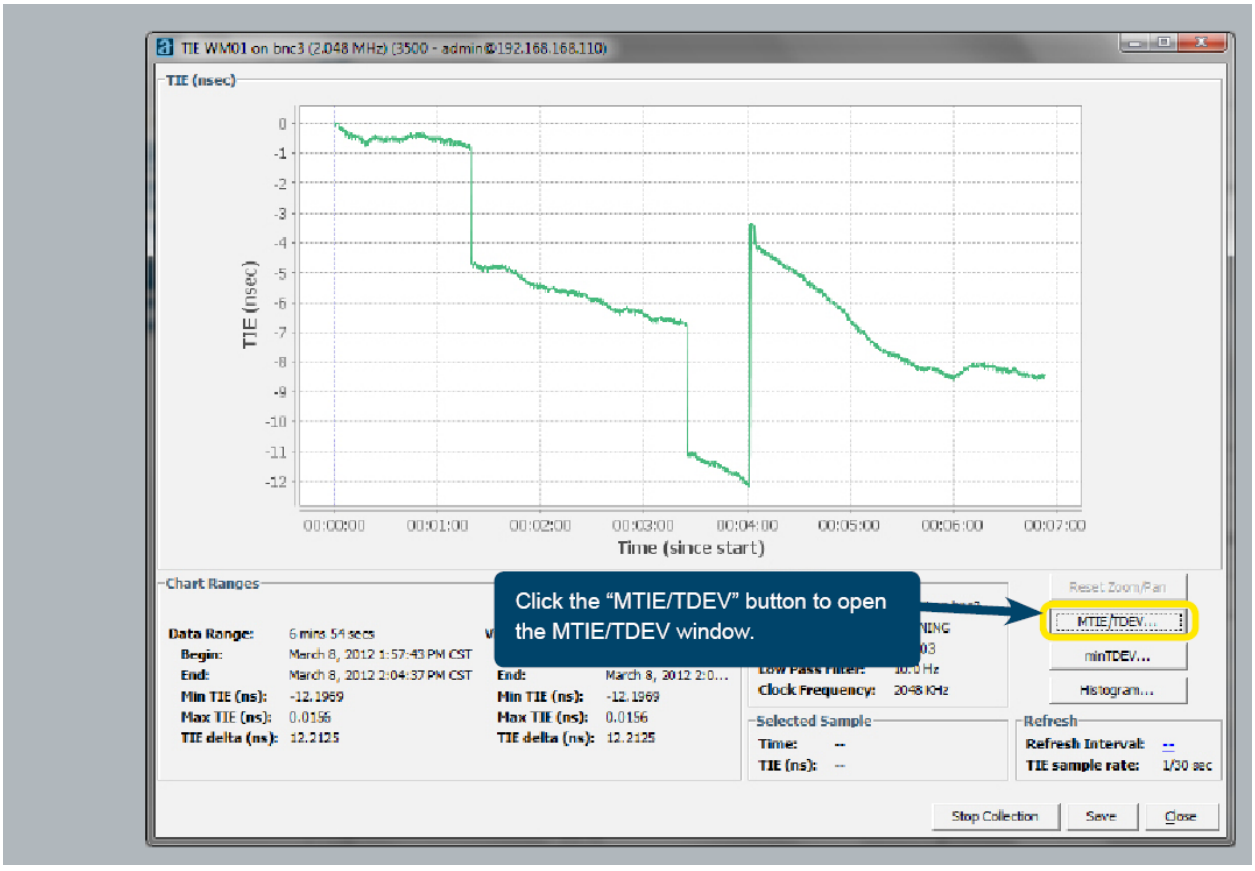

Figure 28: Selecting MTIE/TDEV

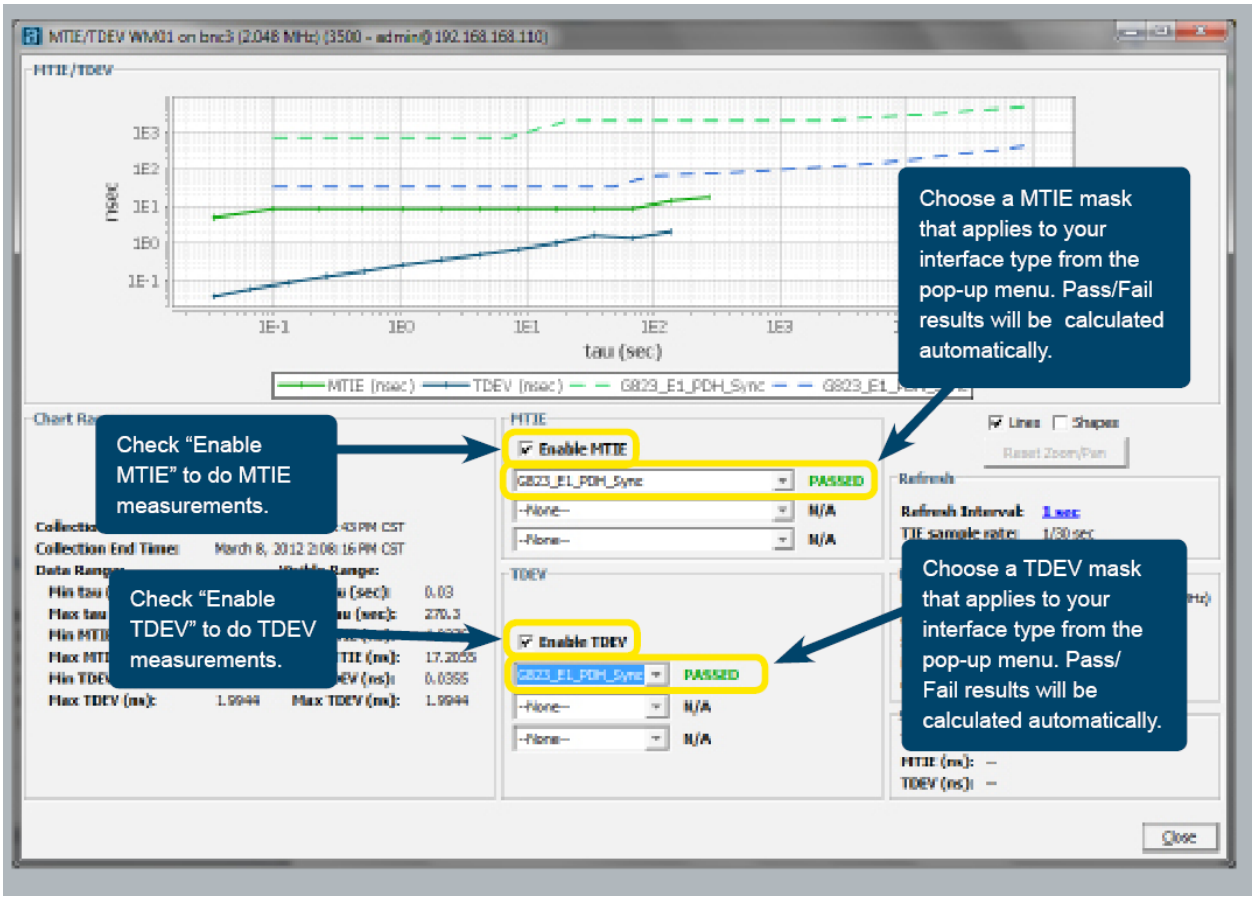

Figure 29: Viewing MTIE and TDEV Results

2) Play the impairment using Network Playback while keeping the TIE window open (recording TIE). You can also monitor the MTIE/TDEV results during the test.

Figure 30: Selecting Network Playback

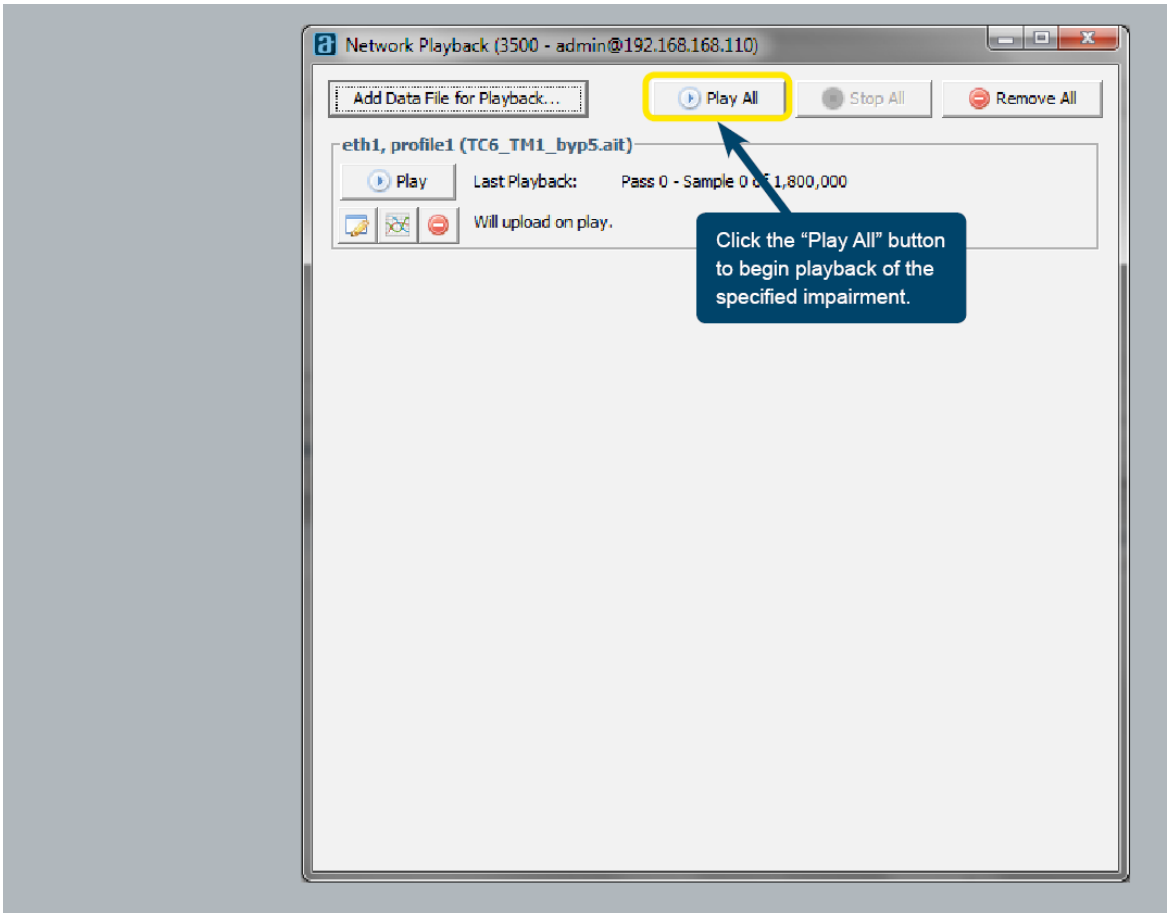

Figure 31: Playing the Impairment File with Network Playback

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Results

1) Each test case includes an impairment that is specified for a certain length of time, ranging from a few minutes to several hours. The result data (TIE) must be collected during the duration of the impairment. Once the impairment for the particular test case finishes, evaluate the frequency accuracy and stability in the MTIE/TDEV window. The graphs for MTIE and TDEV are plotted against the selected masks and pass/fail indication is provided for each mask that is selected.

Note: you must begin recording TIE data before you begin the impairment. Do not close the TIE window for the duration of the test. Once you close the TIE window, the Ixia Anue 3500 will stop collecting the necessary TIE data for the results.

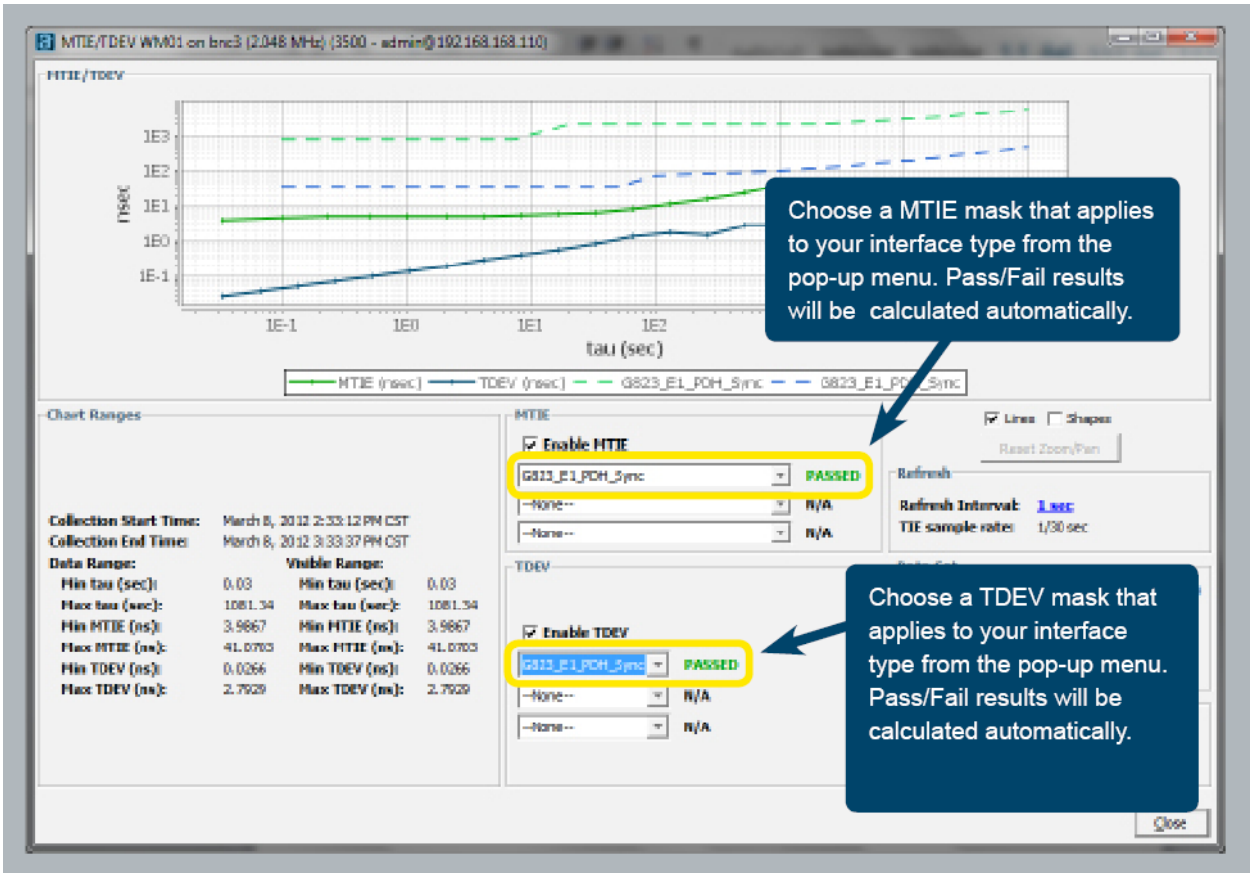


Figure 32: Viewing Results in the MTIE/TDEV Result Graphs Window

2) Evaluate the maximum frequency offset. Typically, the frequency offset is measured in terms of the MTIE value at a tau of 1 second. This can be evaluated in the MTIE/TDEV window by clicking the cursor on the MTIE plot at the tau closest to 1 second (1.02 seconds).

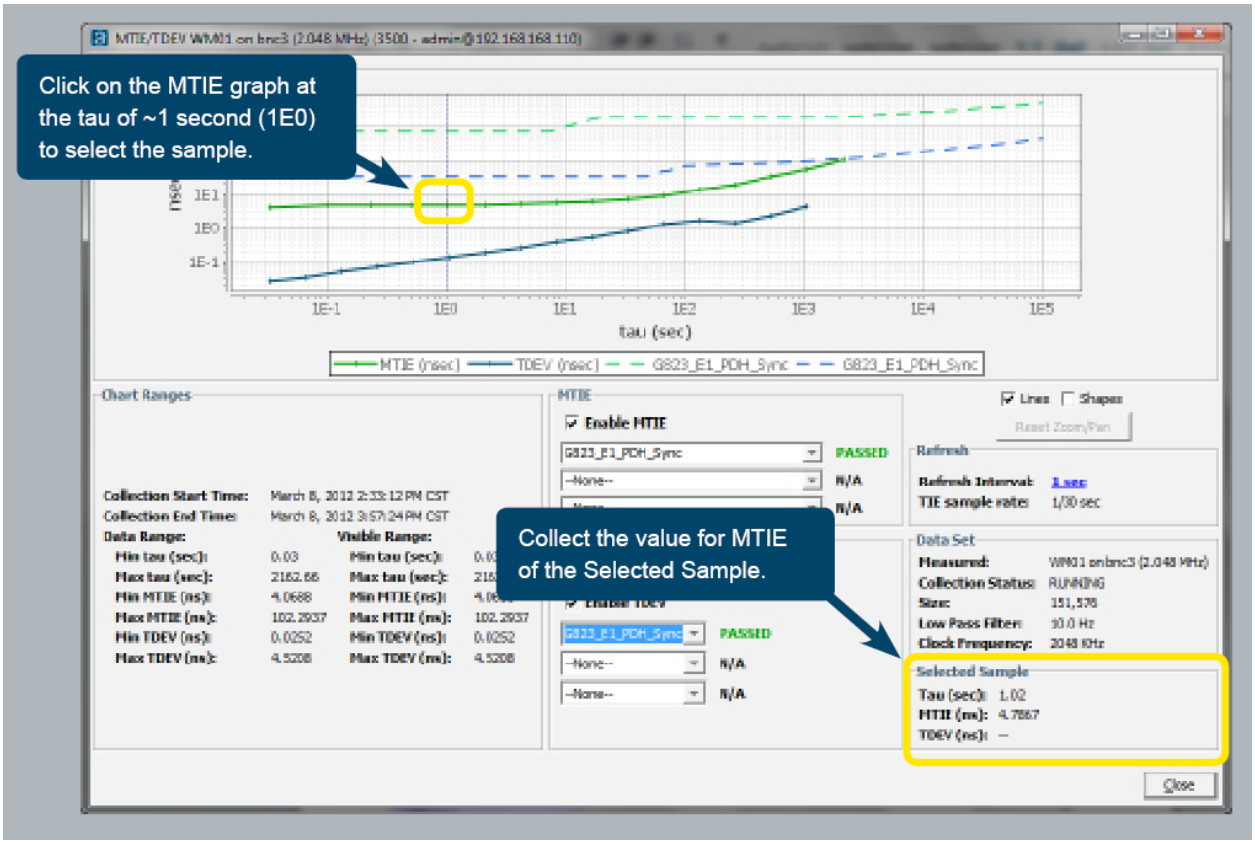


Figure 33: Determining Frequency Offset at 1 Second

The MTIE is indicated in ns (nanoseconds). Frequency offset is typically expressed in ppb (parts per billion). The number of nanoseconds of MTIE at one second of tau is equivalent to ppb frequency offset. For example, in this measurement, the frequency offset is 4.7867ppb.

The maximum frequency offsets are defined by the relevant standard which applies to the interface type. For example, ITU-T G.823 Table 14 defines the maximum frequency offset at traffic interfaces for E1.

G.8261 Test Cases 1-17 with CES

Timing over Packet networks may utilize Circuit Emulation Services (CES). CES utilizes equipment known as Interwork Framework devices (IWF) to transport TDM interface traffic such as T1 or E1 across asynchronous Ethernet packet networks.

TDM circuits send traffic at a constant frame rate from one interface to the next. Since these frames are sent at a constant known rate, it is not necessary to use timestamps to recover the clock. While the CES traffic is synchronous by nature, the intervening Ethernet packet network used for CES between the IWF devices is asynchronous, and therefore the quality of frequency synchronization must be tested. The IWF devices (DUT) may have physical clock interfaces or may provide the clock along with data on the encapsulated TDM stream.

Testing of CES is essentially the same as PTP / IEEE 1588 testing with very minor variations, mostly with regard to how traffic is classified. The testing is accomplished by measuring the recovered clock or PDH interface on the slave DUT while the specified impairment is being introduced between the master and slave IWF device

For additional details see ITU-T G.8261, Appendix VI Measurement guidelines for packet-based methods.

Test Setup

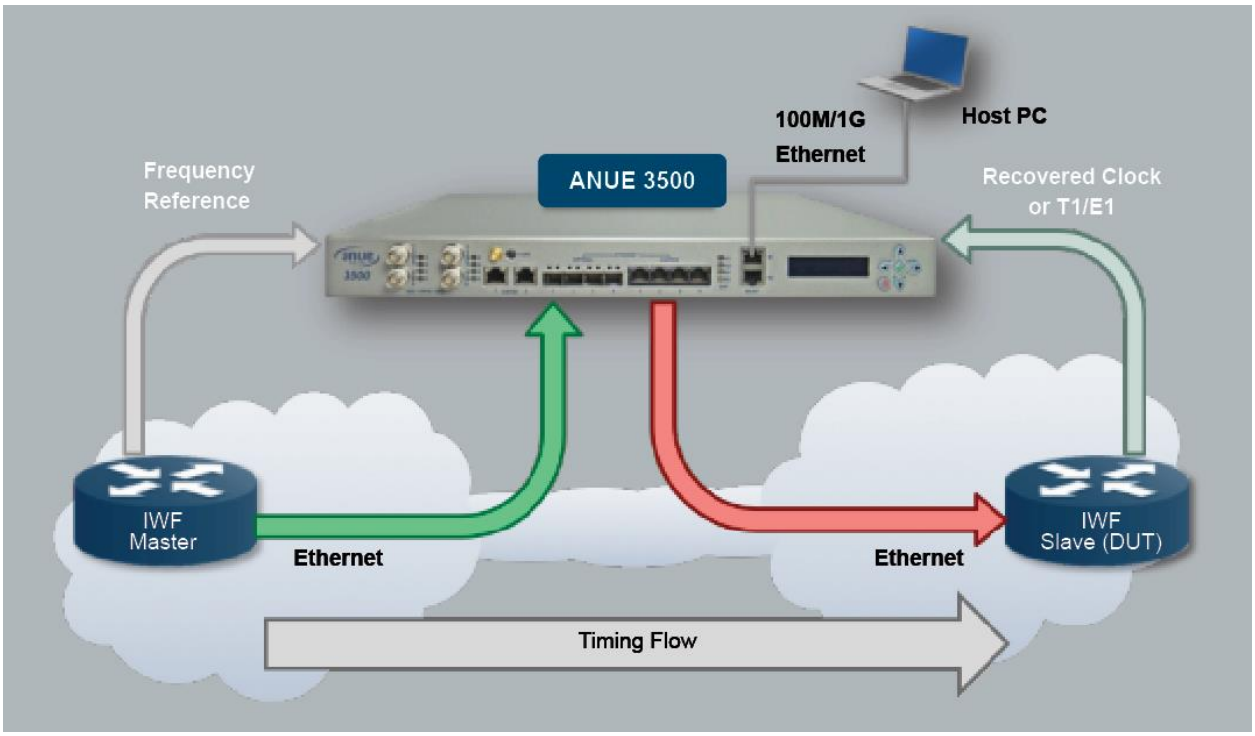


Figure 34: G.8261 Test Setup

1) Follow the test setup steps in Section 5.1 with the following variations:

Configure Network Profiles for each port used in the test to match the CES packets. Configure the classifier for CES for both eth1 and eth2. Note: you must perform this procedure for both the port connected to the DUT slave IWF as well as the port connected to the Master IWF.

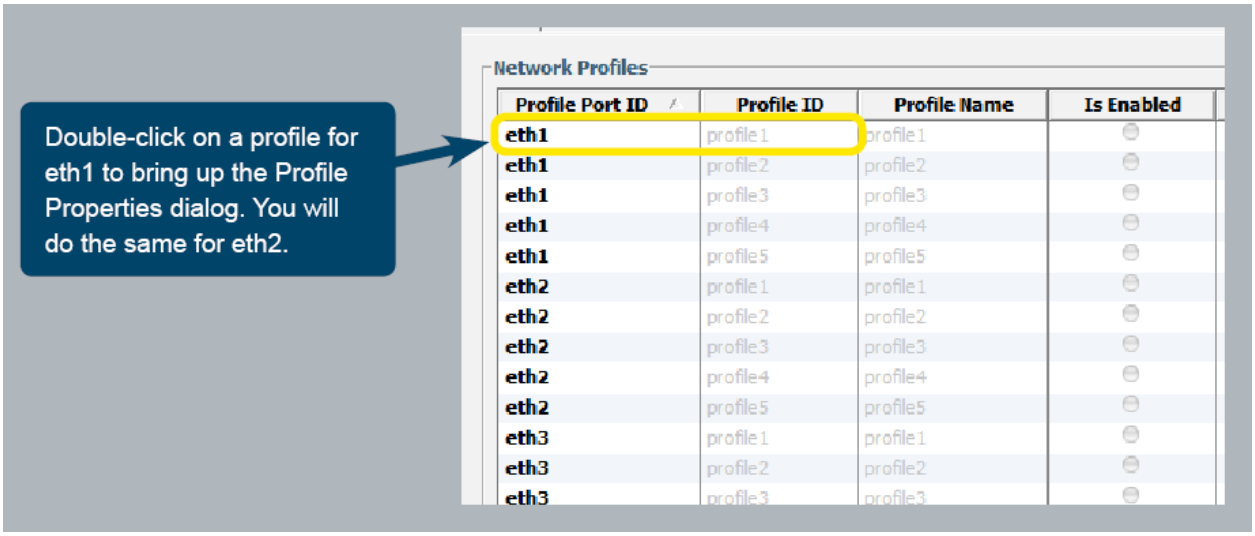


Figure 35: Selecting the Network Profile

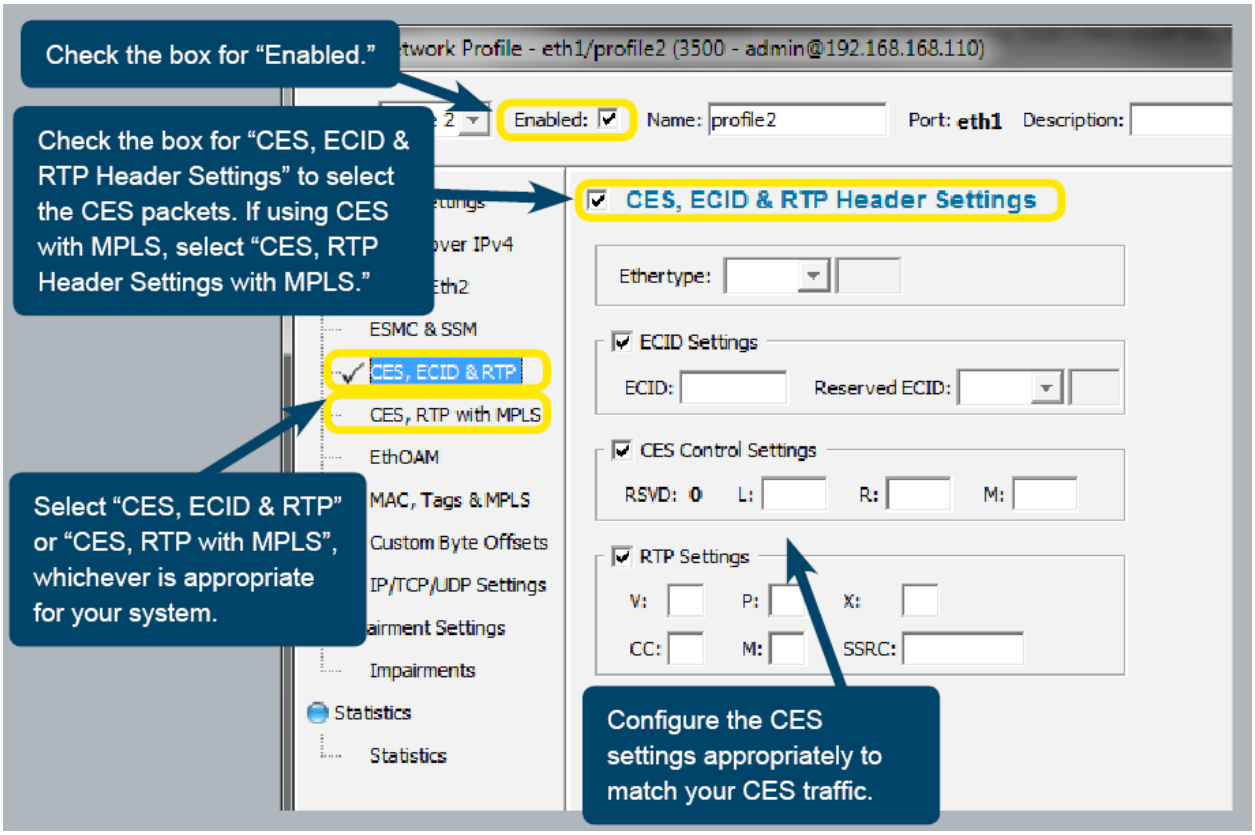


Figure 36: Configuring the Network Profile

Appendix A – Alternate Test Configurations

Some alternate configurations or variations of ToP networks may be tested with the 3500. The following sections describe some examples of methods of testing ToP networks that are not specifically covered by G.8261 or other standards.

Boundary Clock

Boundary Clocks are PTP devices that have a slave port from which they recover a clock. They also have one or more master ports that provide PTP timestamps for downstream devices using the clock recovered from the slave port. These devices may introduce non-linear timing impairments that resemble PDV when introduced into a network. It is important to measure this PDV-like effect in order to characterize a Boundary Clock and consider its impact on a timing network.

Boundary Clocks may also have recovered clock interfaces such as T1/E1 or 2.048MHz that provide the recovered clock. In that scenario, these recovered clock interfaces may be measured and the boundary clock is treated as an ordinary clock or slave clock for the purpose of evaluating recovered clock accuracy. However, the impairment created on the master ports should still also be evaluated independently from the frequency accuracy.

Note: This testing requires that the Ixia Anue 3500 have two Ethernet port pairs for a total of four Ethernet ports.

- **Boundary Clock Test Setup**

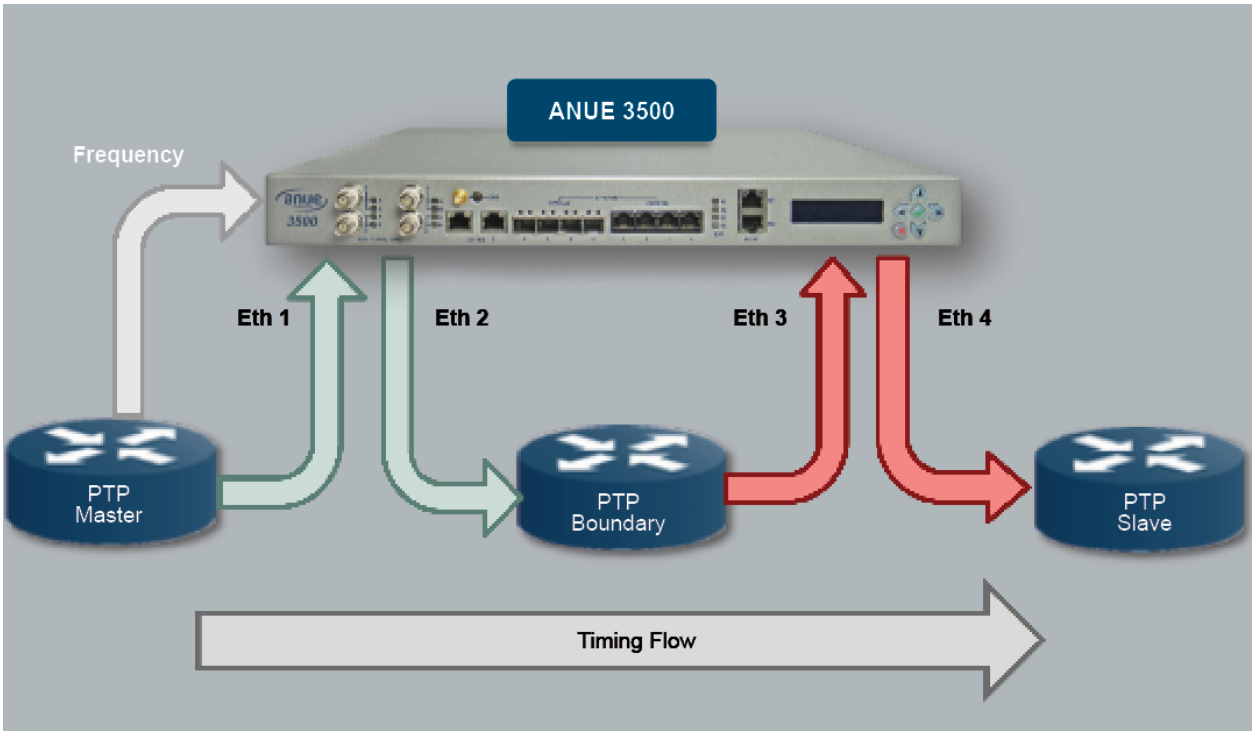


Figure 37: Boundary Clock Test Setup

1) Connect the DUT Boundary Clock, Grand Master clock and PTP Slave Clock to the Ixia Anue 3500 as shown in the test setup drawing:
   a) Connect the Ixia Anue 3500 Eth1 interface to the Grand Master Clock or PTP Master Ethernet interface
   b) Connect the Ixia Anue 3500 Eth2 interface to the DUT Boundary Clock's slave interface
   c) Connect the Ixia Anue 3500 Eth3 interface to the DUT Boundary Clock's master interface
   d) Connect the Ixia Anue 3500 Eth4 interface to the PTP Slave interface

Note: Any mixture of 1G optical or copper, or 1G and 10G interfaces is supported. For example, the Grand Master to DUT can be connected on 10G and the DUT to slave can be connected on 1G, etc.

2) Configure two port-pairs on the Ixia Anue 3500 for "Inline" mode, and if using 1G dual-media ports, configure for the correct media type and speed (copper or fiber, 100M or 1G) using the Ixia Anue 3500 Control Panel Ports tab. Double-click one of the ports in the port-pair that is connected between the Grand Master Clock and the DUT Boundary Clock. This will bring up the Ethernet Port Property dialog.

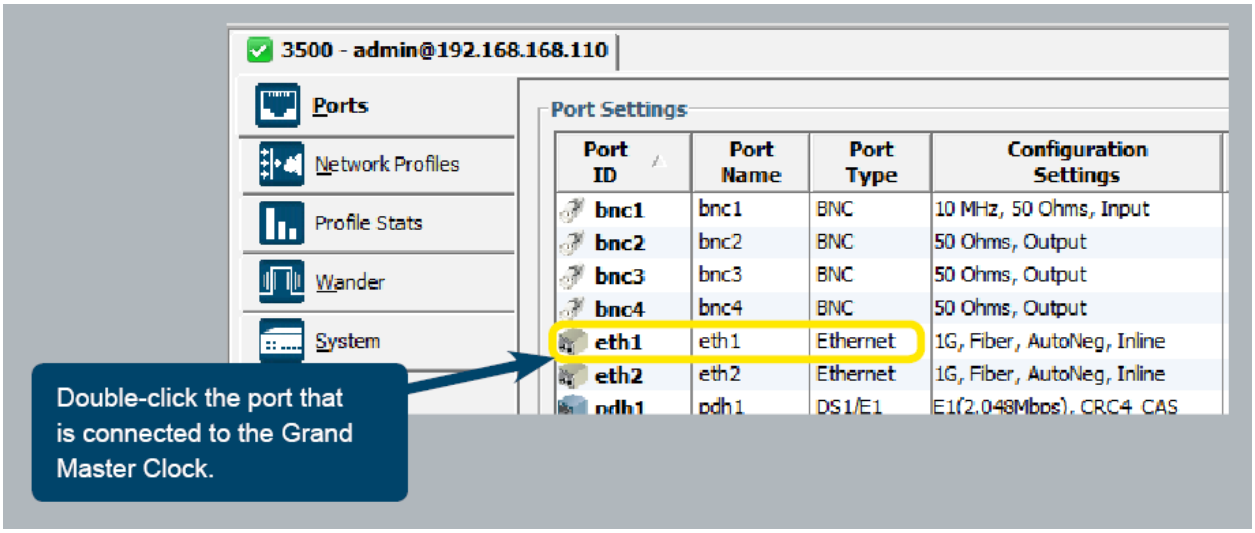


Figure 38: Selecting the Ethernet Port Connected to the DUT

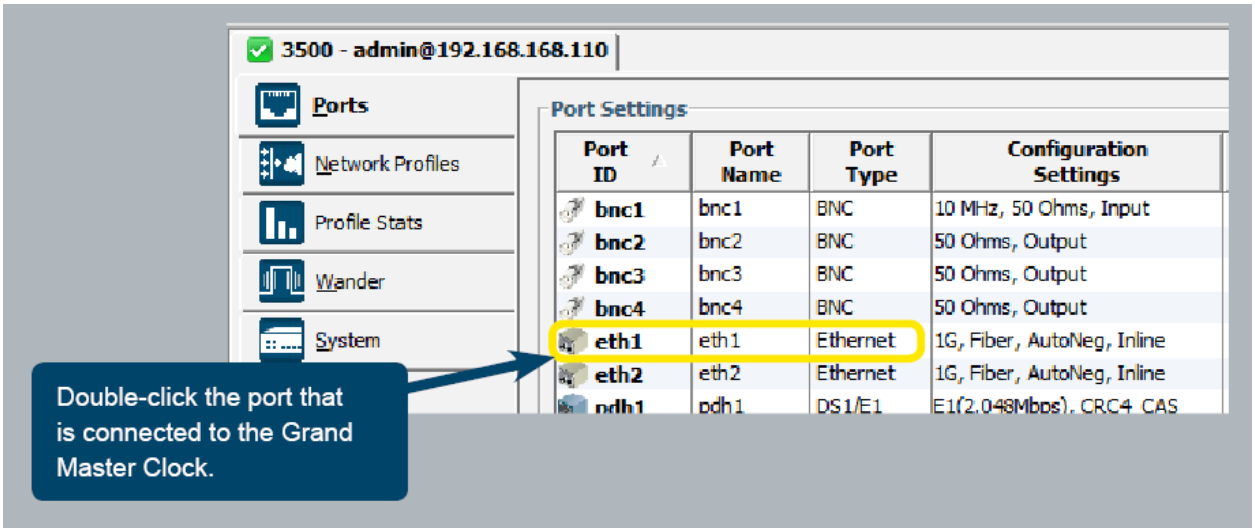


Figure 39: Configuring the Ethernet Port Pair

Repeat this process for the port-pair that is connected between the DUT Boundary Clock and the Slave Clock.

3) Configure Network Profiles for each port used in the test to match the PTP packets. Configure the classifier for PTP for the port connected to the Grand Master Clock (e.g. eth1) and also for the port connected to the master port side of the Boundary Clock DUT (egg. eth3). Note: you must do this procedure for both the port connected to the DUT as well as the port connected to the Grand Master Clock.

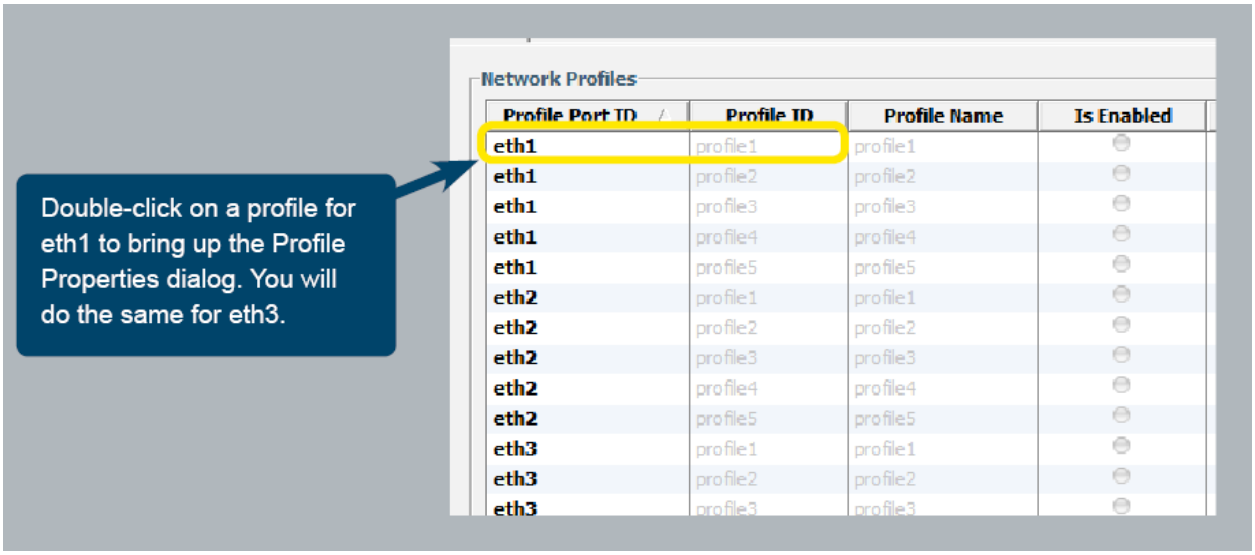


Figure 40: Selecting the Network Profile

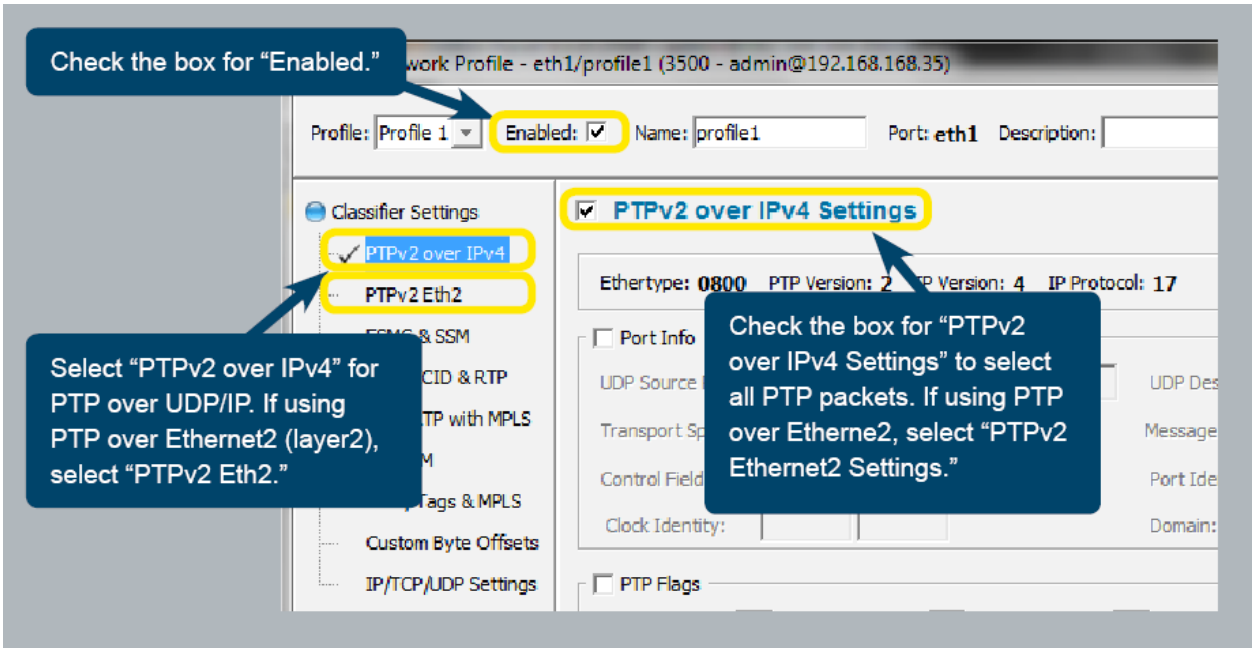


Figure 41: Configuring the Network Profile

- **Test Steps**

1) Begin live PDV on both eth1 and eth3 profiles in the Network Profile window

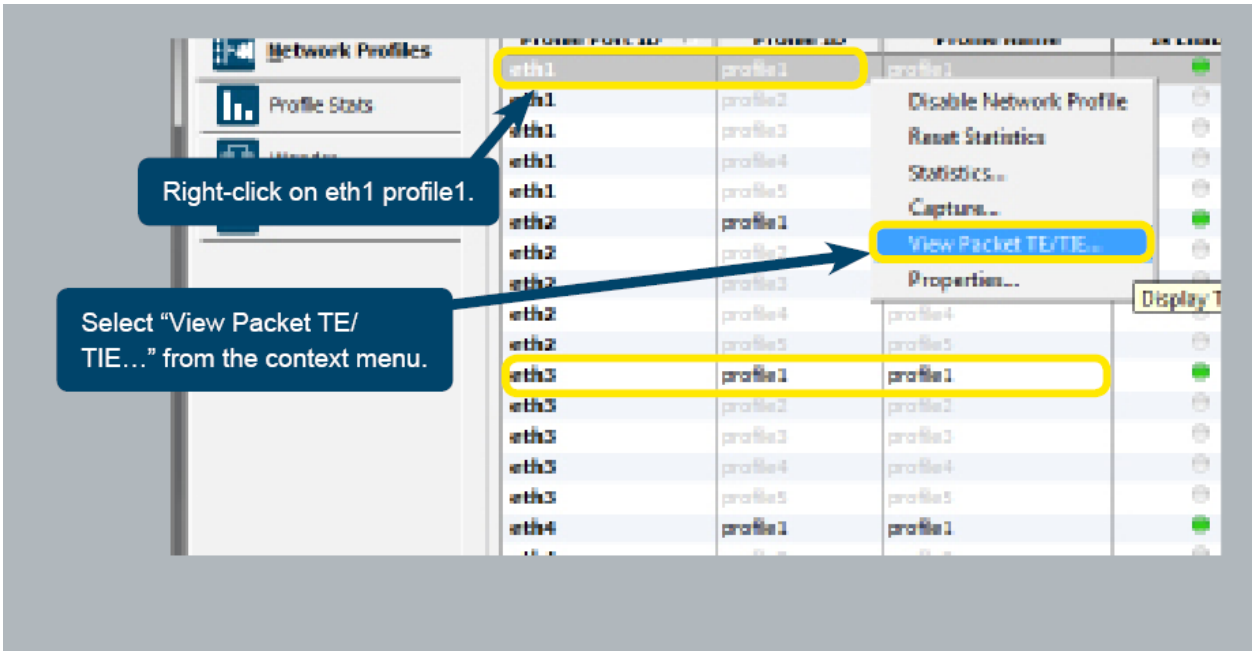


Figure 42: Beginning View Packet TE/TIE

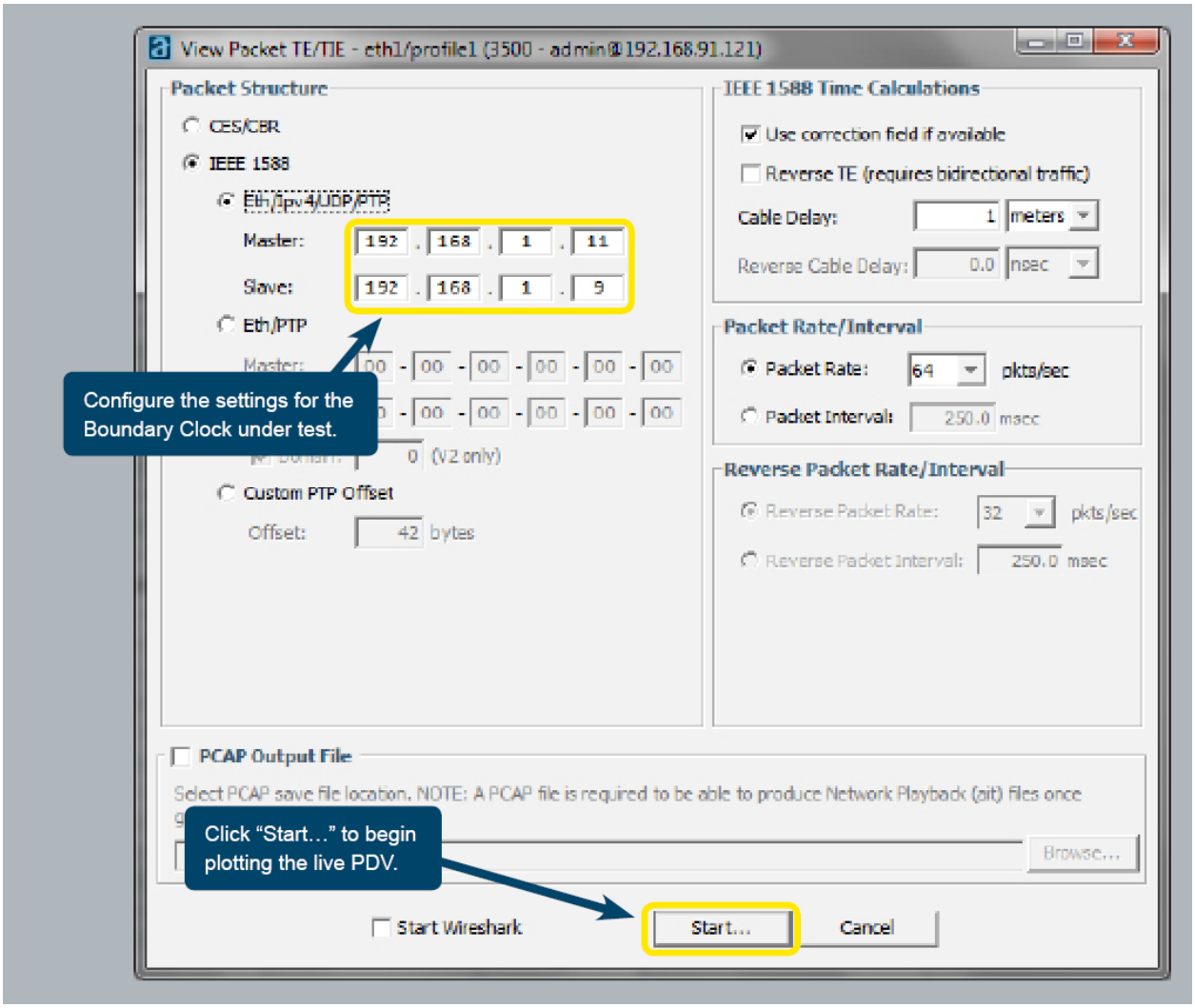


Figure 43: Configuring Live PDV

Repeat the same process for eth3 profile1.

- **Results**

1) Review the PDV on eth3 compared to eth1's PDV. This indicates the insertion properties of the Boundary Clock.

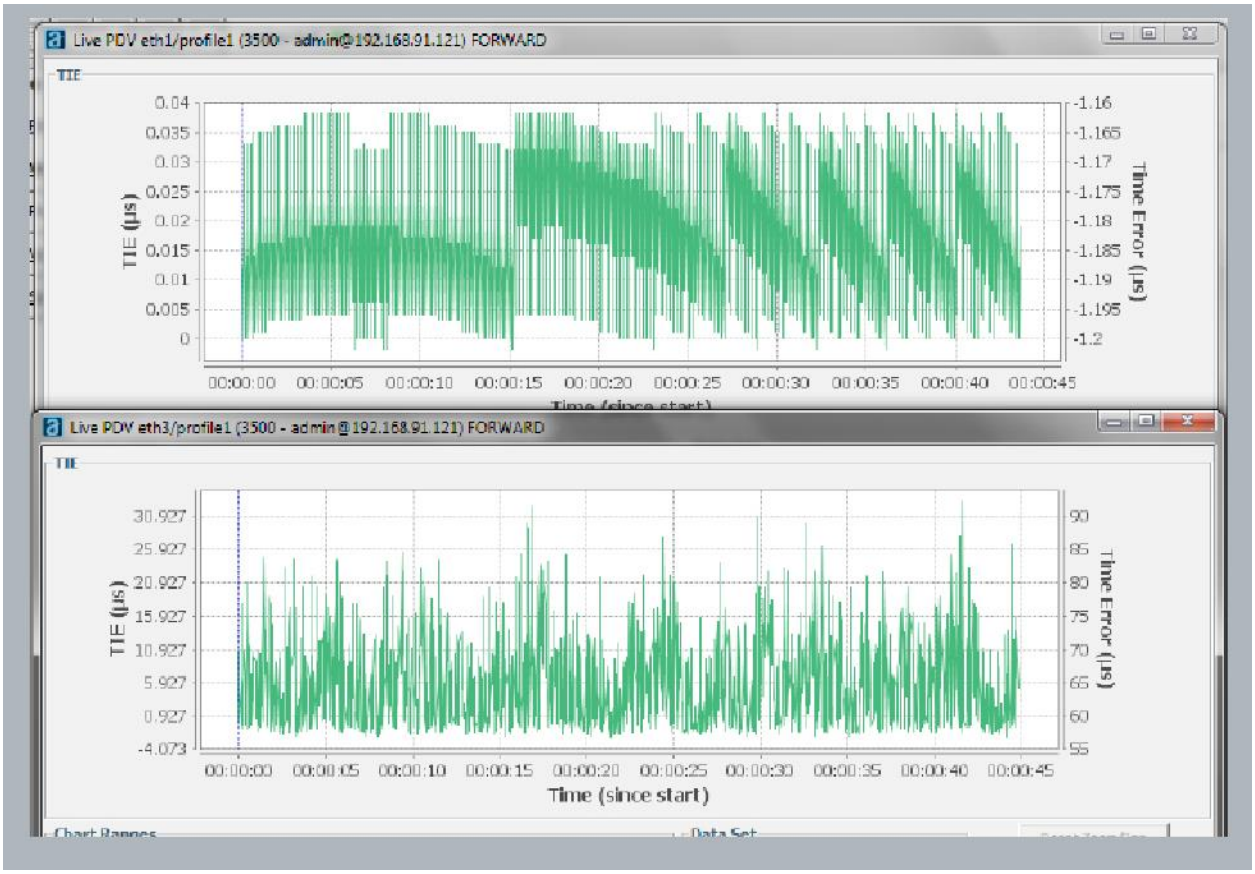
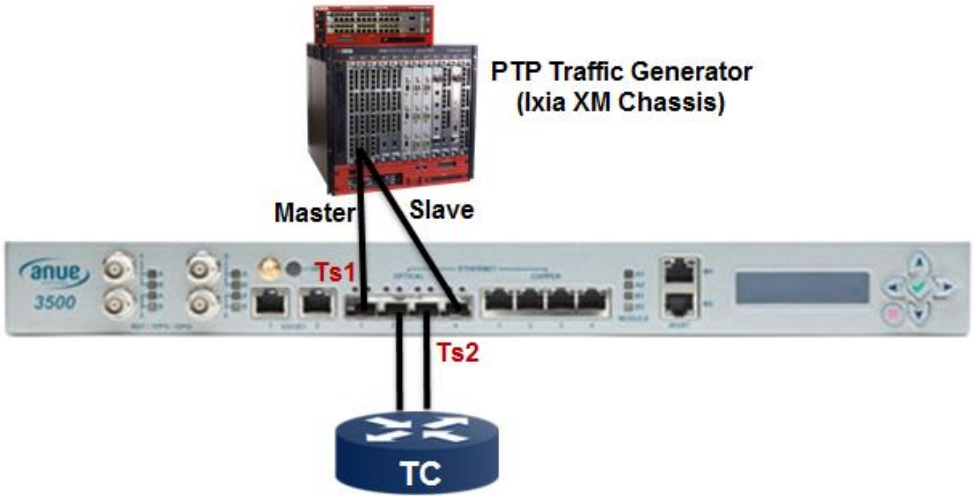


Figure 44: Comparing PDV of a Boundary Clock

Transparent Clock

Transparent Clocks are PTP devices that forward PTP packets from one port to another while updating the PTP packet's correction field. The correction field is updated by adding the residence time (time the packet spends inside the transparent clock) to the current value of the correction field. This value allows the slave clock to compensate for the PDV caused by all the transparent clocks in the PTP network path. It is important to measure the accuracy of the correction field as updated by the transparent clock. Note that this testing requires that the Ixia Anue 3500 have two Ethernet port-pairs for a total of four Ethernet ports. During analysis, PTP packets are monitored at two locations: "pre-clock" and "post-clock" as shown in the example setup in the figure below.

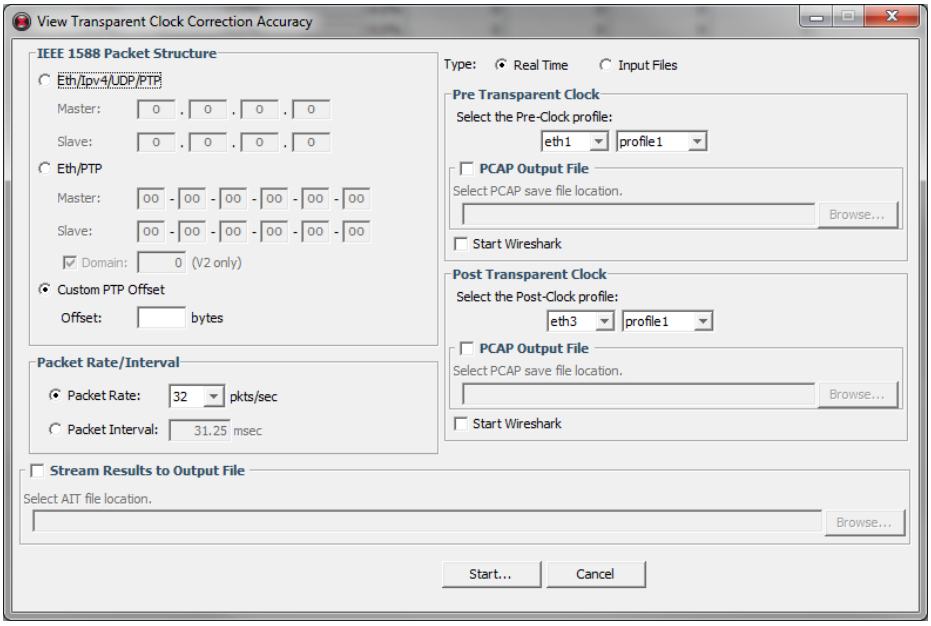


Residency Time = Ts2 – Ts1
Time Error = Residency Time – Correction

To analyze transparent clock accuracy, follow the steps below.

1. In the 3500 Control Panel, select the Network Profile or Profile Stats view. The Transparent Clock Analysis icon appears in the icon toolbar.

2. Click the Transparent Clock Analysis icon. The Transparent Clock Analysis dialog displays.



3. At the left side of the dialog, select the IEEE 1588 Packet Structure (Eth/Ipv4/UDP/PTP or Eth/PTP) that matches your traffic and then configure the Master and Slave addresses.

   Domain: Select and configure the domain option if you are using IEEE1588 version 2 and have a group of clocks.
   Custom PTP Offset: If the PTP layer starts in a non-standard location within the Ethernet frame, select this option. Enter an offset in bytes that indicates where the PTP layer starts.

4. Configure the expected "Packet Rate" or "Packet Interval" of the traffic.

5. At the right side of the dialog, configure the traffic that will be monitored by selecting the "Real Time" option.

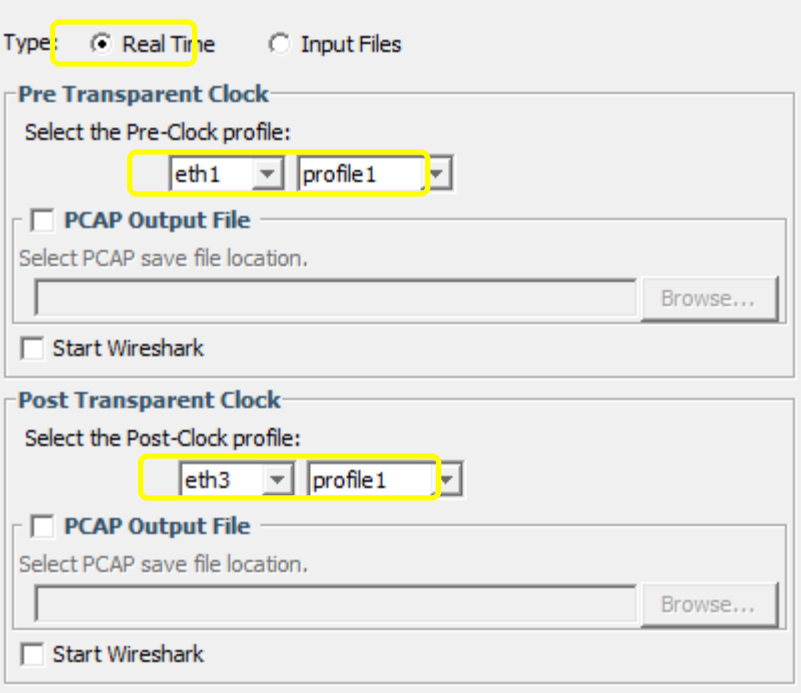


Figure 45: Transparency Clock Accuracy Real Time Options

6. Under the "Pre Transparent Clock" section of the dialog, select the Pre-Clock Ethernet port and Network Profile. Disregard the other settings in this section; please see the I*xia Anue 3500 User Guide* if you would like more information about these options.

7. Under the "Post Transparent Clock" section of the dialog, select the Post-Clock Ethernet port and Network Profile. Disregard the other settings in this section; please see the I*xia Anue 3500 User Guide* if you would like more information about these options.

8. At the bottom of the dialog, select and configure "Stream Results to Output File" if you want to save the results to an AIT file.

9. Click **"**Start" to begin Transparent Clock accuracy testing.

10. A graph of the accuracy data will display as shown in the figure below. In this example, the graph indicates the correction field errors in nanoseconds. An error occurs when a PTP packet's correction field value differs from the Anue 3500 measurement of the packet's residency time. The Data Set area of the window (boxed in red), provides test configuration and status information.

    Note: Starting the analysis in "Real Time" mode requires the buffering of data before data points start appearing on the delay accuracy chart. Because analysis relies on comparing two independent streams of traffic, the actual duration of buffering varies depending on the specified packet rate as well as actual packet rate. A buffering progress status message will display until enough packets have been received to allow for data points to be graphed.

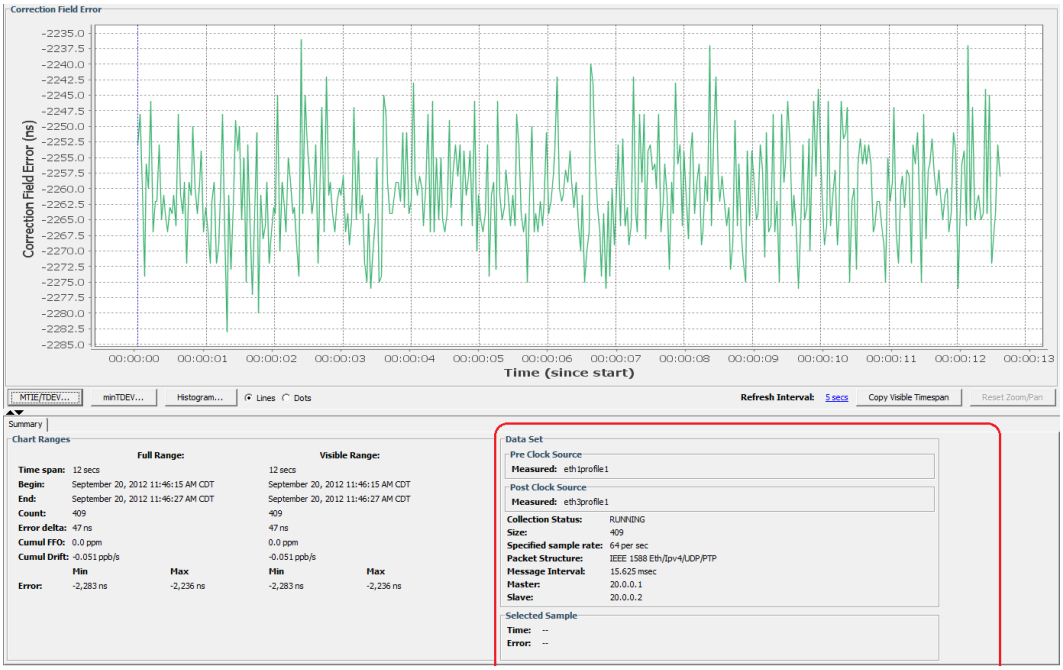


Figure 16: Real Time Transparency Clock Accuracy

G.8261 Testing of Hybrid SyncE & PTP Devices - Ethernet Recovered Clock

Timing over Packet networks may use a combination of PTP and Synchronous Ethernet (SyncE), where frequency and phase synchronization are delivered across a packet network using PTP, and the frequency recovered at the slave (or boundary clock) is delivered on SyncE interfaces. Testing these hybrid networks is accomplished by measuring the recovered clock on the slave DUT on the SyncE interface while the specified packet impairment is being introduced between the Grand Master and the DUT.

- **Test Setup**

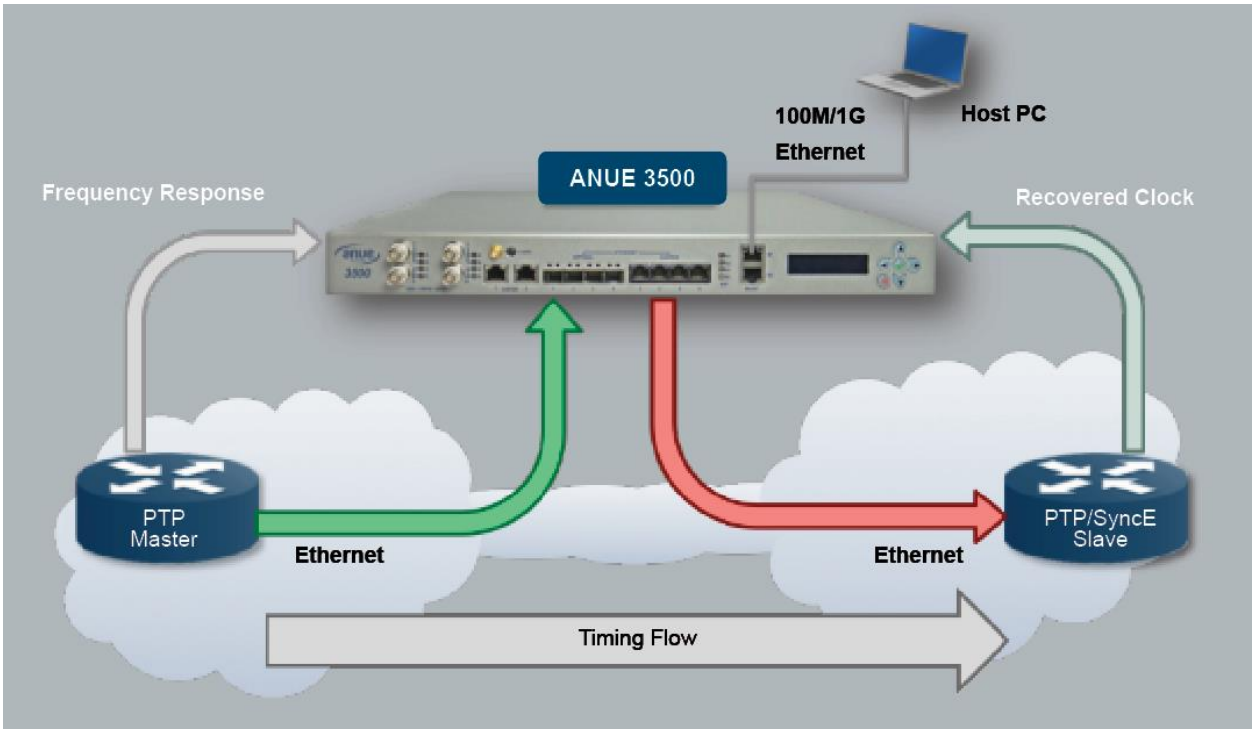


Figure 47: G.8261 / SyncE Test Setup

Testing and setup is identical to section 5.1 G.8261 Test Cases 1-17 with PTP / IEEE1588, with the exception of the choice of recovered clock interface, and the selection of masks for measurement of this clock. Complete the setup steps from section 5.1 with the following variations.

1) The Slave's recovered clock is measured on the Ethernet interface that is connected between the 3500 and the DUT. Select a Wander Measurer from the Ixia Anue 3500 Control Panel's Wander tab to measure the DUT's Ethernet interface. Configure the Wander Measurer for the correct interface.

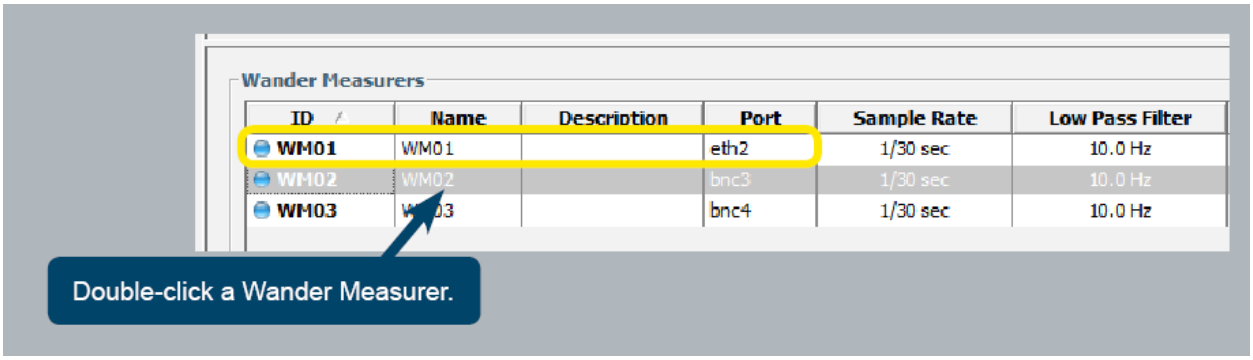


Figure 48 Selecting a Wander Measurer from the Wander tab

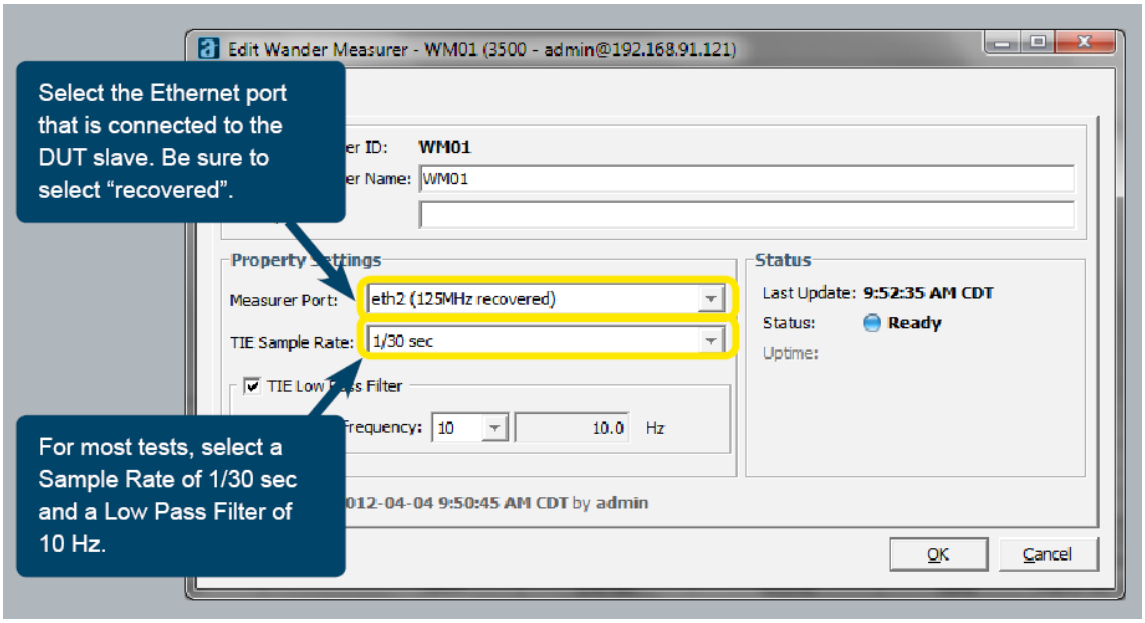


Figure 49: Editing the Wander Measurer

2) The PTP Slave DUT may take up to an hour or longer to become synchronized with the Grand Master Clock. You can identify synchronization by monitoring the DUT's Ethernet clock TIE graph, and also by monitoring the user interface for indication of synchronization.

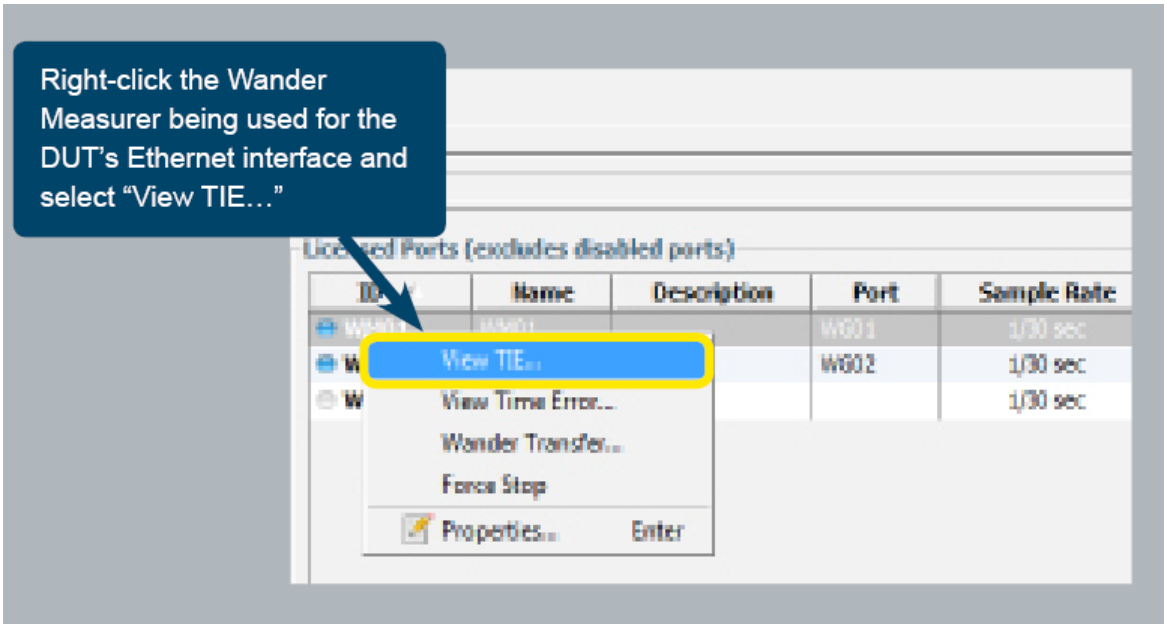


Figure 50: Selecting "View TIE..." for the Wander Measurer

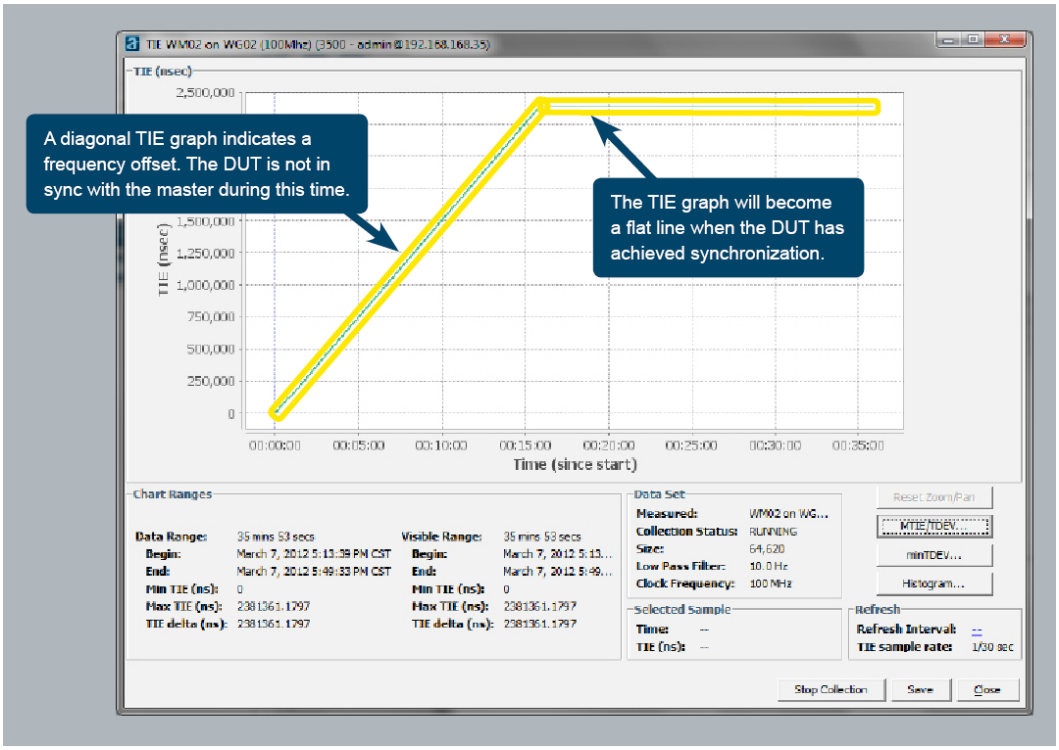


Figure 51: Monitoring TIE during Synchronization Phase

3) Once the DUT is in sync with the Grand Master, close the TIE window and restart the TIE measure

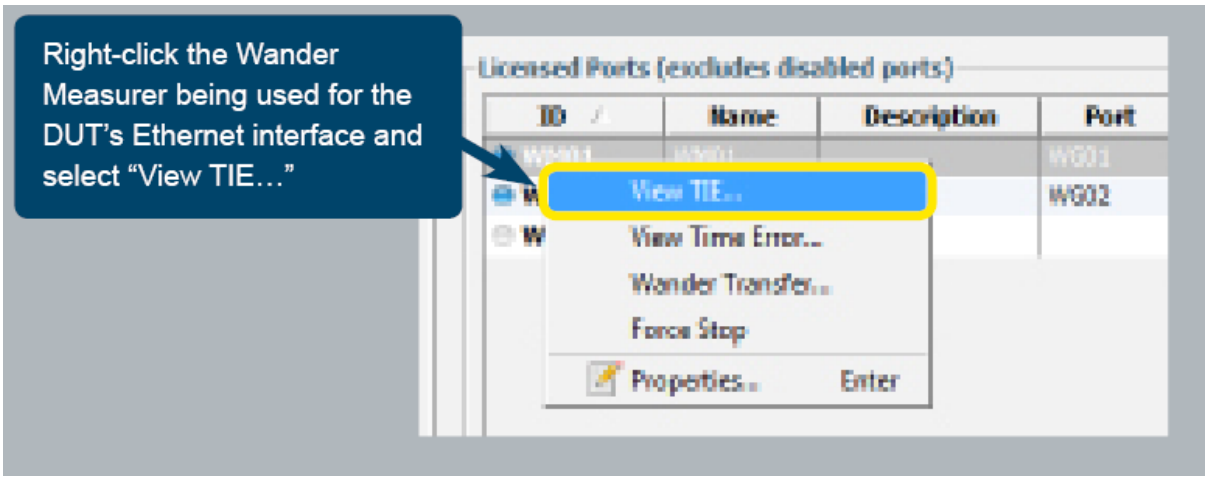


Figure 52: Starting the TIE Measurement

- **Test Steps**

Test steps are the same as in section 5.1 G.8261 Test Cases 1-17 with PTP / IEEE1588

- **Results**

Results are the same as in section 5.1 G.8261 Test Cases 1-17 with PTP / IEEE1588, only differing in the masks chosen for SyncE measurements in the MTIE/TDEV window.

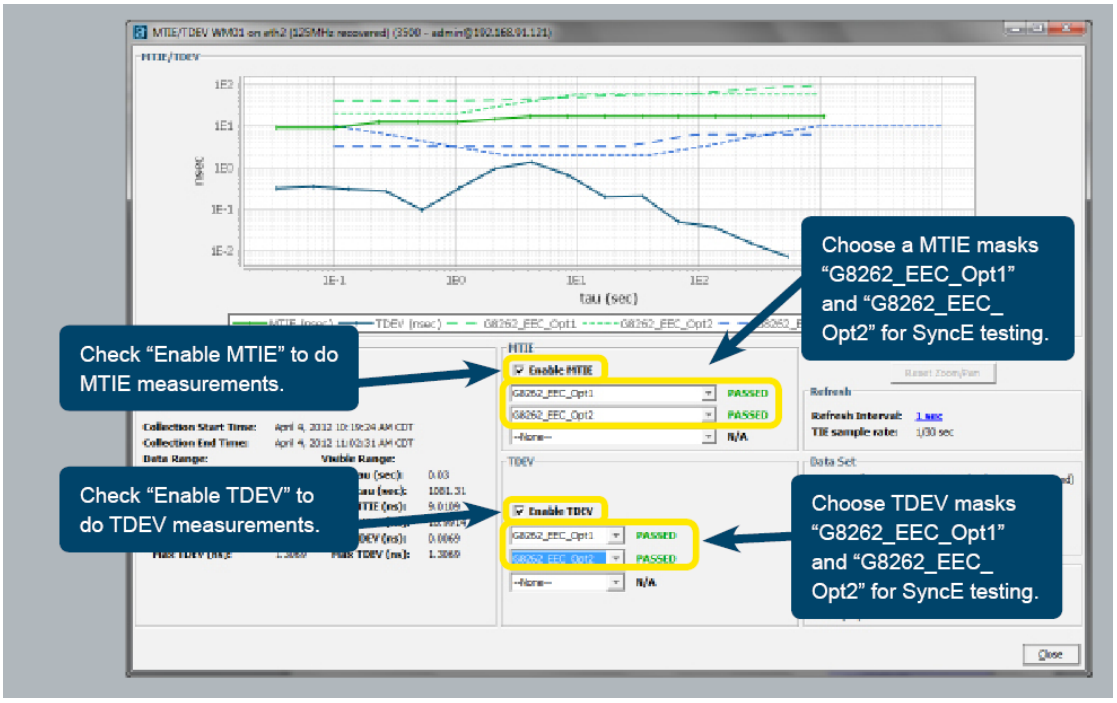


Figure 53: Viewing MTIE and TDEV Results

General Testing of Hybrid SyncE & PTP Networks – SyncE Frequency & PTP Phase

Synchronous Ethernet (SyncE) may be used to deliver frequency synchronization on networks in conjunction with PTP used for Phase or Time of Day delivery. In this type of network, only Ethernet interfaces are used. The Ixia Anue 3500 supports testing a variety of network combinations, with physical layer (SyncE) and packet layer (PDV) measurement and impairment conducted simultaneously.

- **Test Setup**

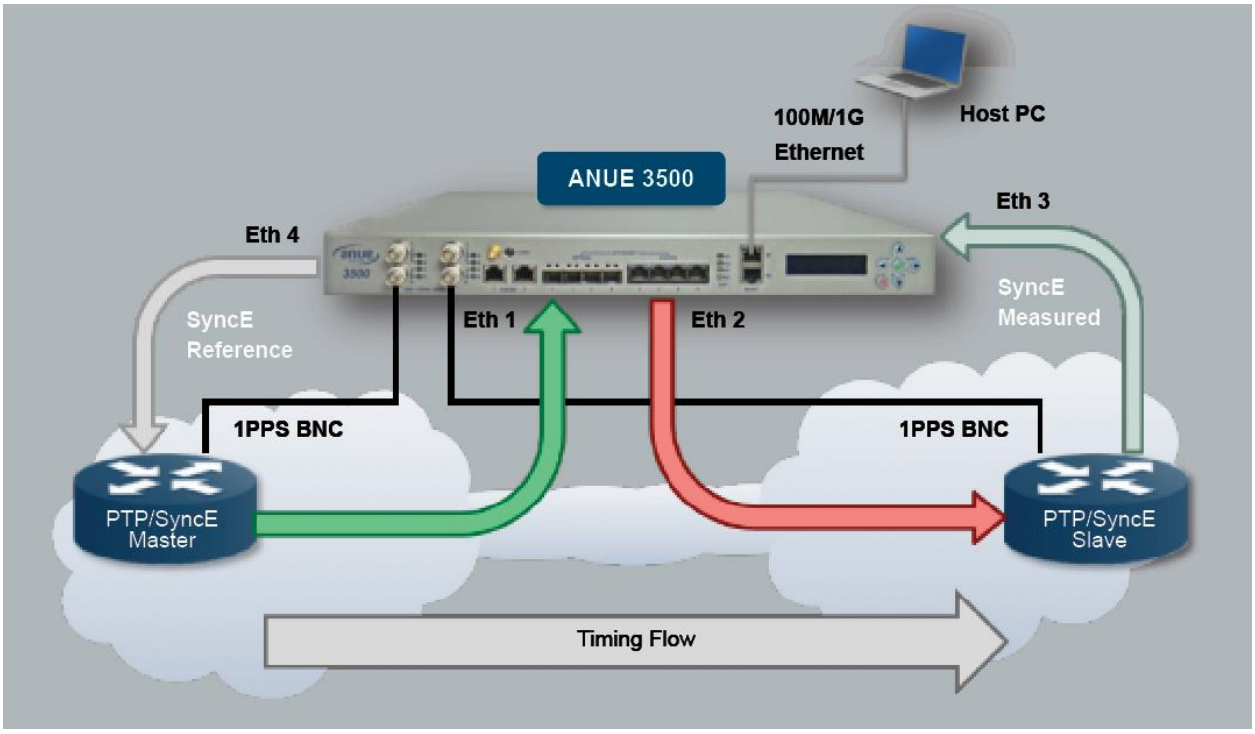


Figure 54: G.8261 / SyncE Test Setup

1) Connect the 3500 to the PTP/SyncE devices as shown in the diagram. Note that this testing requires two pairs of Ethernet ports. Eth4 from the 3500 should be connected to a SyncE slave port on the Master device in order to provide a frequency reference over SyncE
2) Connect the 1PPS output from the Master and slave DUTs to BNC ports on the Ixia Anue 3500. Configure these BNC ports for Receive 1PPS, and configure the cable delay to match the length of cable connecting to each port

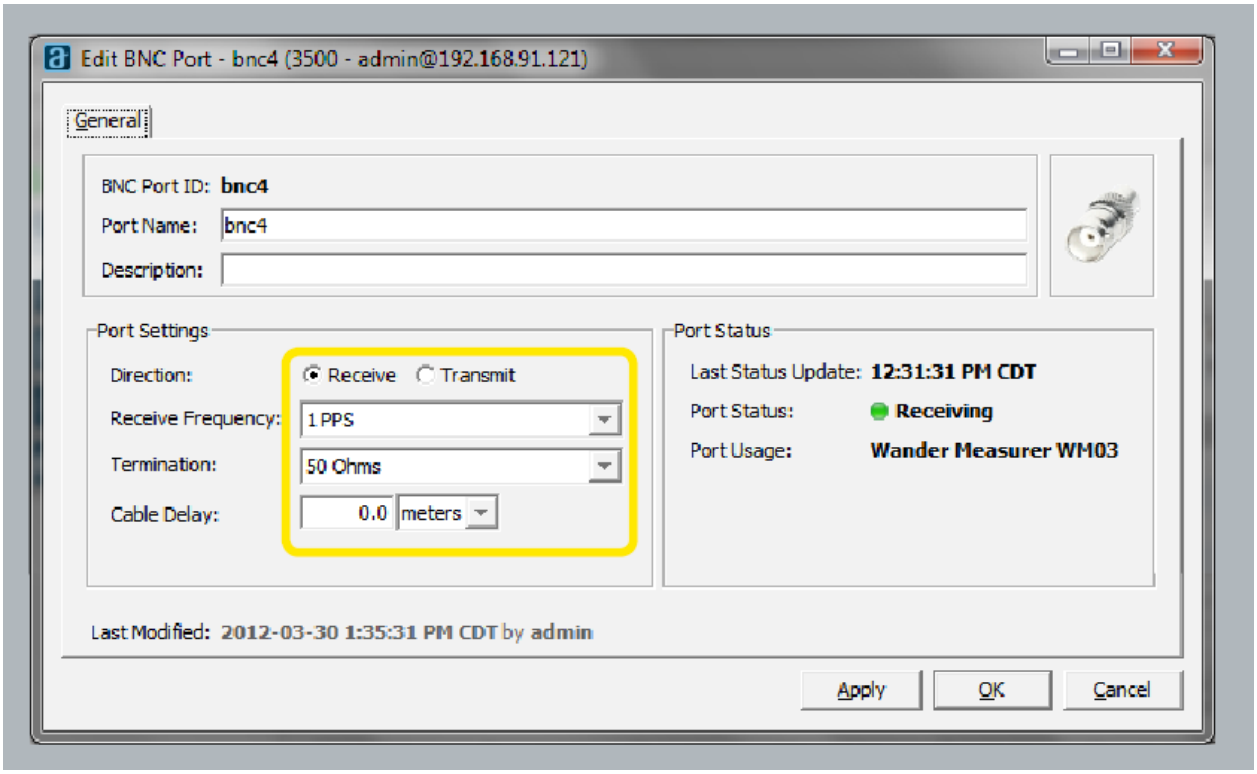


Figure 55: Configuring 1PPS Test Interface

3) Port Pair PP-B is used to provide SyncE frequency reference to the Master device, and to measure the SyncE recovered clock on the slave.

   a) Set Port Pair PP-B to “Endpoint” mode, and set the Reference Clock for WG01

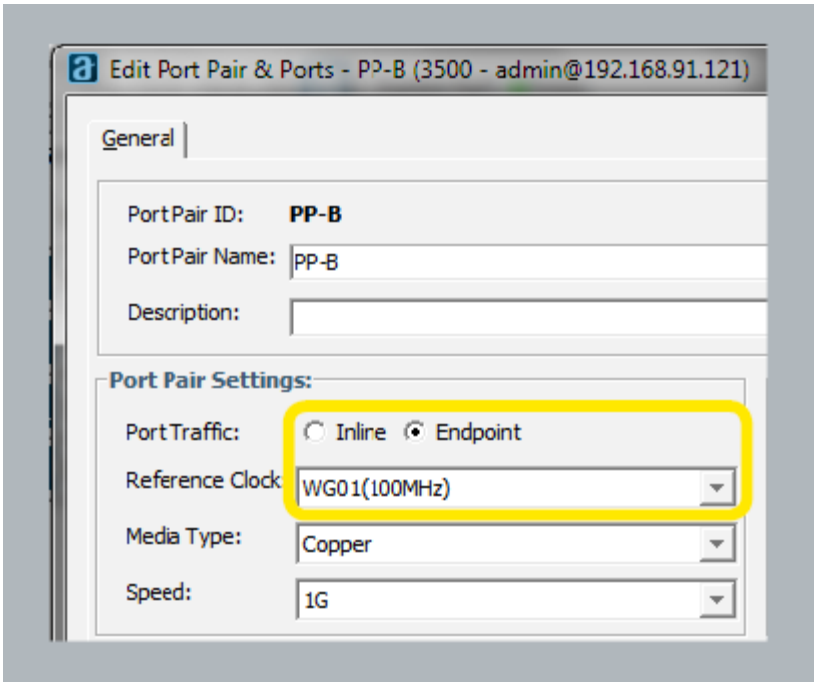


Figure 56: Selecting Endpoint Mode

b) Configure ESMC Generation on Eth4 – configure to match the requirements of the DUT Master port connected to Eth4 in order for the DUT Master device to become slave

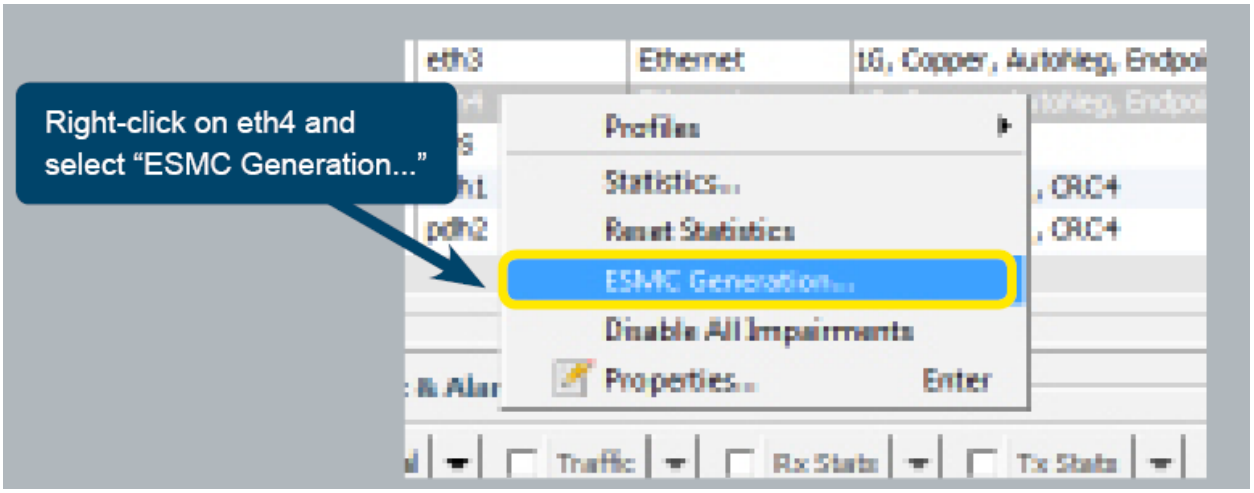


Figure 57: Selecting ESMC Generation

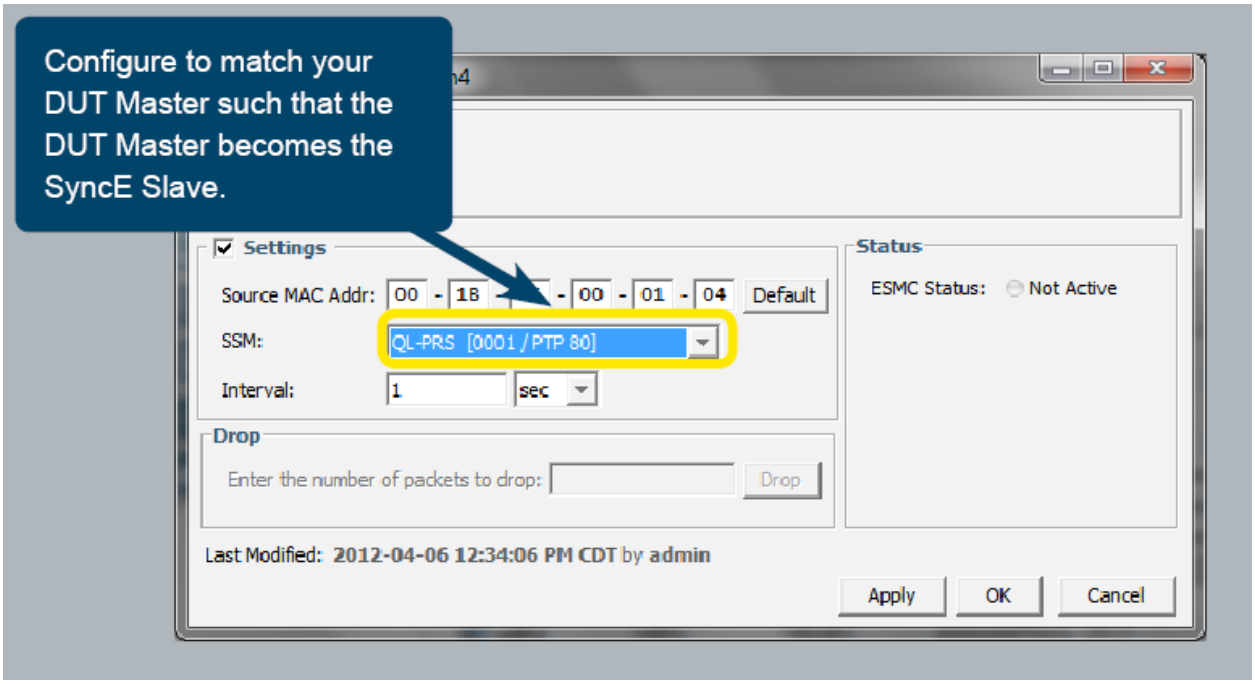


Figure 58: Configuring ESMC Generation

c) Select a Wander Measurer from the Ixia Anue 3500 Control Panel's Wander tab to measure the DUT's Ethernet interface. Configure the Wander Measurer for the correct interface.

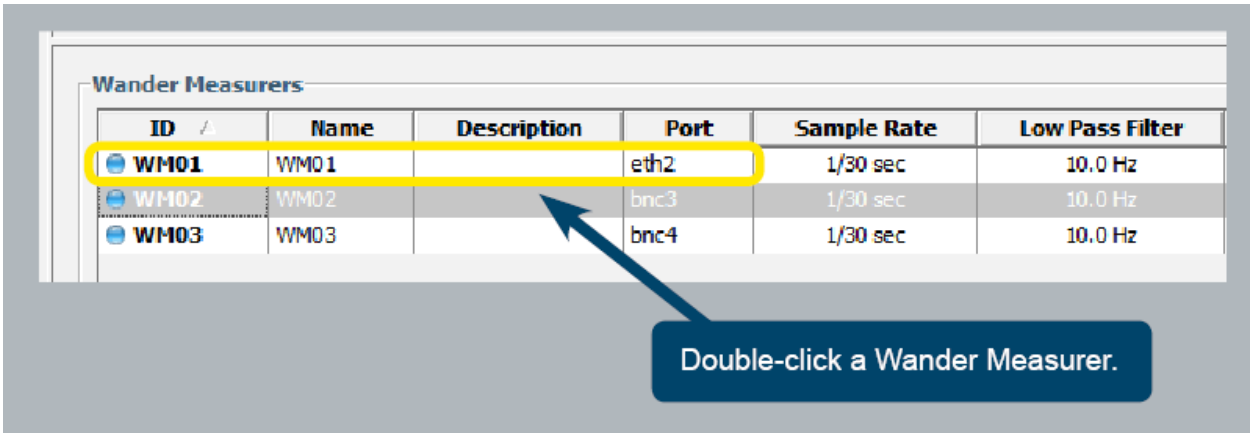


Figure 59: Selecting a Wander Measurer from the Wander Tab

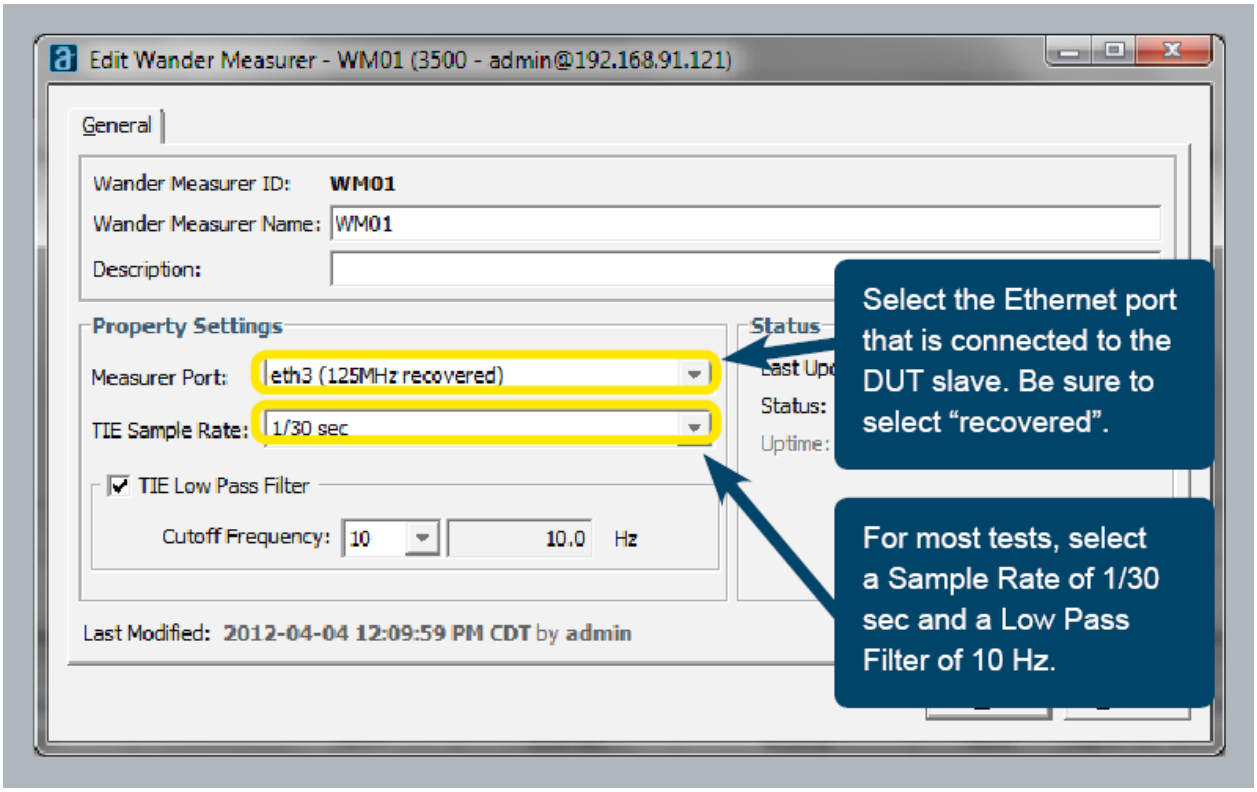


Figure 60: Editing the Wander Measurer

4) Port Pair A is used to apply packet-layer impairment (PDV) between the Master and Slave. Follow steps 6-7 from Section 5.1.1 to set up PDV Impairments.
5) With Synchronous Ethernet, the DUT Master and Slave should be synchronized in a matter of seconds.
6) Packet-layer impairment can be introduced on the PTP packet stream that is used to deliver time of day and phase. Configure PDV impairments as in steps 6-7 of section 5.1.1
7) Once synchronization is complete, measure the Time of Day error in terms of phase (1PPS) from the Wander view of the 3500 Control Panel.

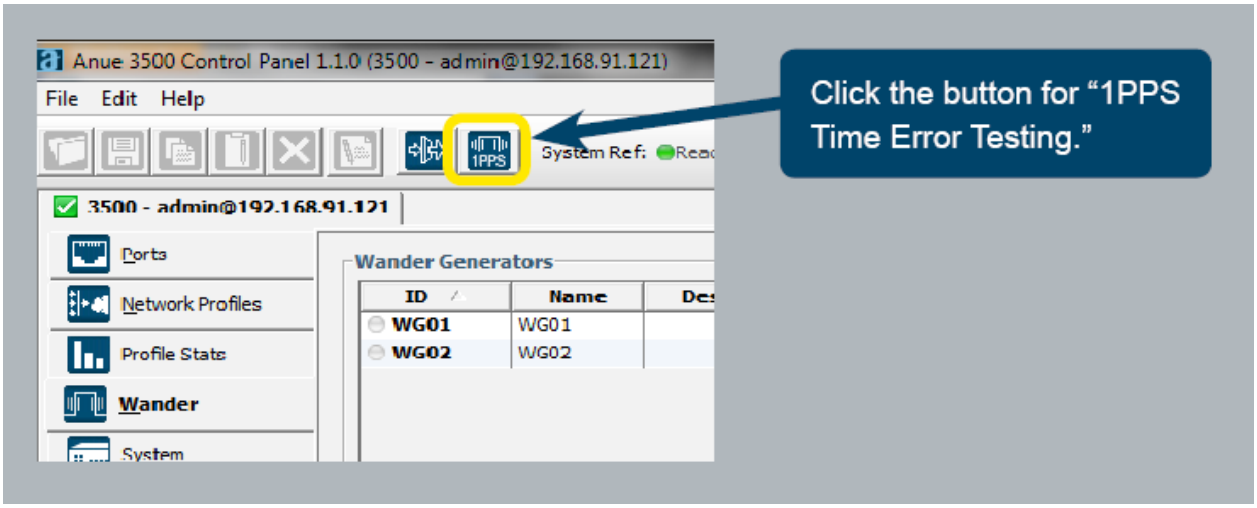


Figure 61: Selecting the 1PPS Time Error Testing Button

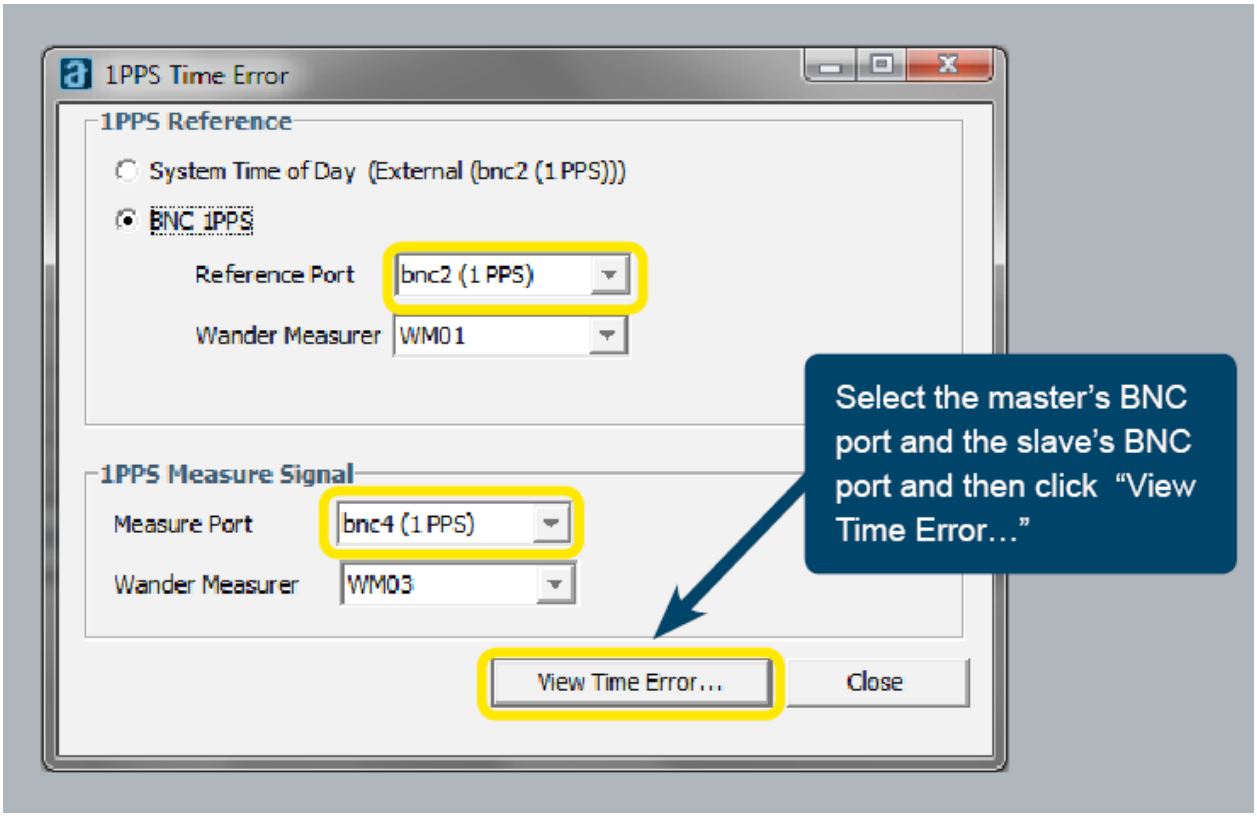


Figure 62: Viewing Time Error on 1PPS Interfaces

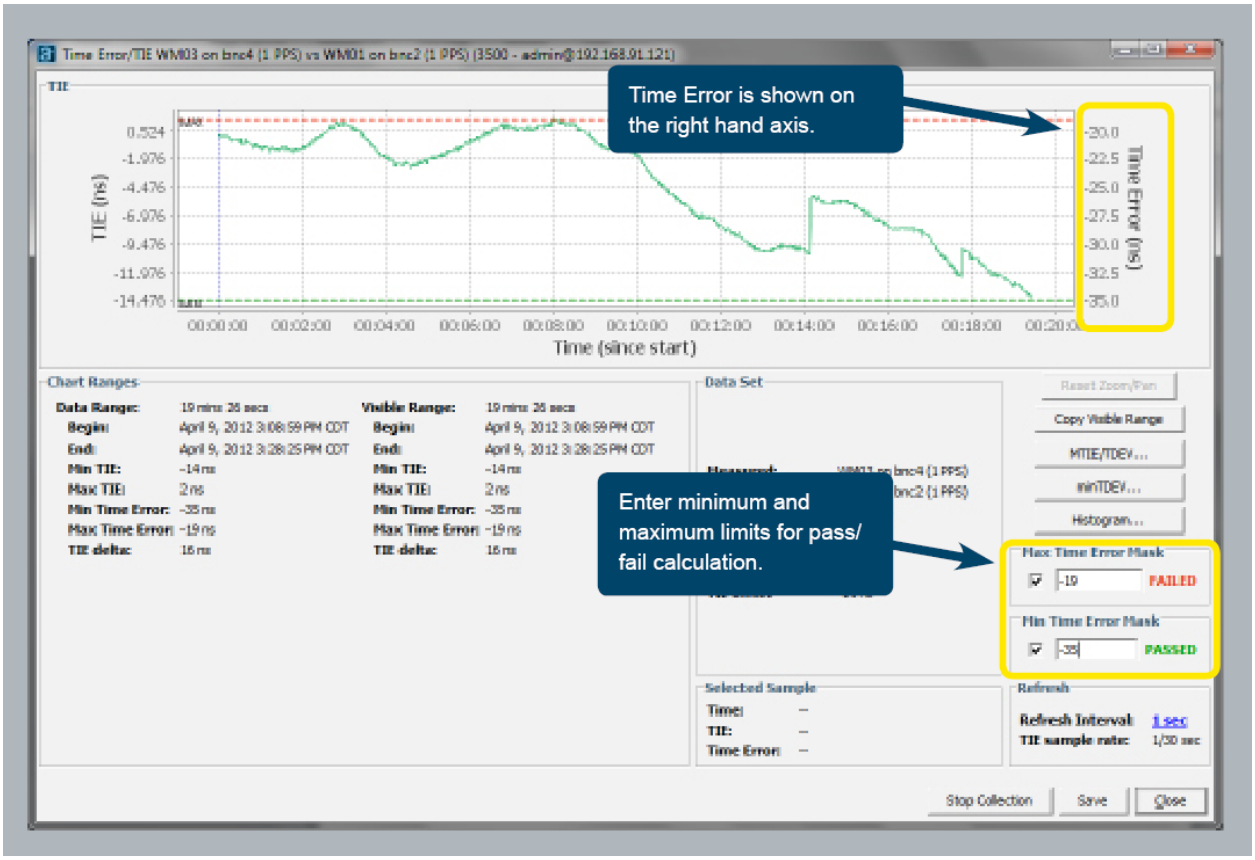


Figure 63: Evaluating 1PPS Time Error

8) While testing Time Error on 1PPS, you can also measure MTIE and TDEV on the recovered clock interface on the slave, whether it is on BNC, PDH interface, or Ethernet. Please see previous test sections for details on configuring measurement of MTIE and TDEV on recovered clock interfaces.

9) While testing PTP and SyncE in hybrid mode, you can simultaneously introduce physical layer impairments on the Ethernet connection between the Master and Slave DUTs. Please see the Application Note Ixia Anue 3500 – Testing SyncE Wander for details on configuring impairments for SyncE testing.