WHITE PAPER

ixia

Testing PTP / IEEE1588 On-Path Support Devices

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Overview

As the demand for advanced mobile broadband services continues to increase, many network providers and carriers are migrating their mobile backhaul networks from legacy synchronous transports such as SONET/SDH and T1/E1 to Carrier Ethernet. Traditional TDM networks provided not only data transport, but also synchronization of frequency.

Synchronization equivalent to what has been provided for TDM networks must be provided on Ethernet networks in order for Ethernet to be used as a replacement for TDM. This must be done without impact to synchronization quality and network performance.

Furthermore, modern wireless networks are demanding time/phase synchronization as well. It is critical to verify synchronization performance of Ethernet network elements prior to deployment.

Three primary methods are used to deliver synchronization over Ethernet:

Synchronization equivalent to what has been provided for TDM networks must be provided on Ethernet networks in order for Ethernet to be used as a replacement--without impact to synchronization quality and performance.

Circuit Emulation Service (CES): TDM frames from T1 or E1 circuits are encapsulated and transported directly over Ethernet, often in pseudowires, over devices known as Interworking Functions (IWF). Normal TDM equipment exists at both ends of the connection. Timing (frequency) is recovered exactly in the same manner as in conventional TDM, given that it is simply TDM traffic that is being transported over an Ethernet pseudowire. The quality of the recovered timing is determined by the IWF and the method(s) used.

IEEE1588 Precision Time Protocol (PTP): A two-way time transfer protocol wherein a Grandmaster clock is synchronized to a high-quality source such as GPS and then generates packets with precise timestamps that are sent downstream to slave devices. The slave devices use these timestamps as well as a delay request and response conversation in order to derive the clock that is supplied to equipment requiring synchronization. Devices between the master and slave clocks may be ordinary switches and routers, or specialized equipment with on-path support, such as Boundary Clocks and Transparent Clocks, that are intended to mitigate the effects of timing impairment introduced by the network between the master and slave.

Synchronous Ethernet ("SyncE"): Uses the bit clock of the Ethernet physical layer to provide frequency synchronization. ESMC frames are sent between the SyncE EEC devices in order to advertise clock quality and other synchronization status messages (SSM).

These different methods may be used independently or in conjunction with one another and hybrid networks that intentionally use more than one technology in order to leverage the strengths of each are increasingly being deployed, notably PTP with SyncE. Network operators and service providers must test their equipment and networks prior to deployment in order to ensure interoperability, applicability of the design for the intended application or purpose, and to maximize revenue and customer's quality of experience.

Likewise, equipment manufacturers must test their equipment prior to presenting it to their customers, the network operators and service providers. Vendors of Ethernet hardware and silicon solutions (PTP-enabled Ethernet PHYs, PTP protocol stacks, etc.) must also test their equipment in order to sell to the equipment manufacturers.

Test laboratories also test solutions in order to establish the quality or applicability of this equipment prior to deployment. Given the tremendous growth of revenue expected in mobile network bandwidth and deployment, comprehensive pre-commissioning testing of the equipment is imperative.

The ITU-T, ETSI and IEEE, among others, provide standards that specify limits and methods of testing for Carrier Ethernet technology. New standards and amendments are being added continuously as development of this technology progresses.

Ixia provides a suite of equipment and applications that are essential in the testing of Synchronization over Ethernet:

InNetwork emulates master and slave clocks and add background traffic for conformance testing of devices or network elements

IxANVL (Automated Network Validation Library) is the industry standard for automated network/protocol validation

Ixia Anue 3500 Performs precise emulation of real-world network impairments such as packet delay variation and wander, and also measures time error, packet delay variation, and physical layer wander as required by ITU-T standards

Challenges Facing Synchronization in Ethernet Networks

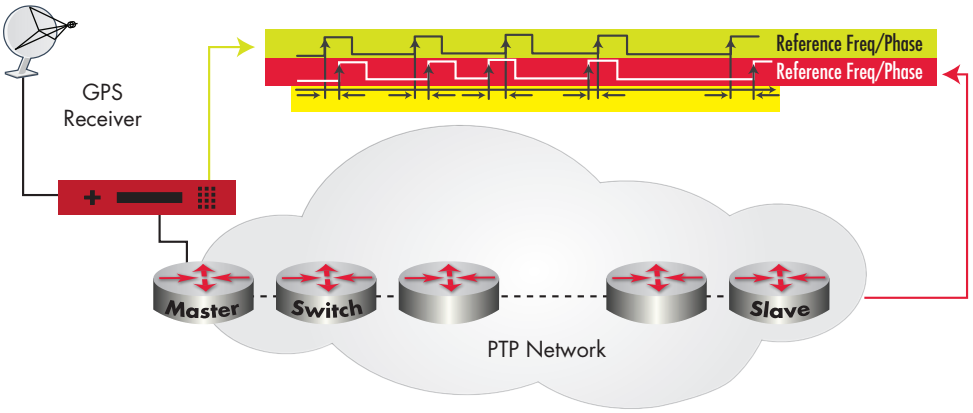


Figure 1 – Synchronization Network Topology

On a PTP network, Time (frequency, phase, ToD) is distributed from the PTP Master and recovered at the slave device for use by remote network equipment. The Ethernet packet network between master and slave may include a number of switches or routers, which handle normal data traffic, traffic requiring synchronization such as CES/pesudowires or VoIP, in addition to PTP traffic.

Traffic congestion, queuing effects, QoS etc. in the packet network between the master and slave device can cause a non-linear timing impairment, known as packet delay variation, or PDV, as well as delay asymmetry. The PTP Protocol relies upon accuracy of time intervals between packets for accurate frequency recovery and delay path symmetry for accurate time synchronization. This variation in delay and any asymmetry affects the quality of synchronization of the slave device.

Boundary Clocks and Transparent Clocks are PTP-aware switches that provide the on-path support required to reduce the effect of PDV and delay asymmetry on a synchronization network.

Given the tremendous growth of revenue expected in mobile network bandwidth and deployment, comprehensive pre-commissioning testing of the equipment is imperative.

Packet Delay Variation: Packet Delay Variation is the variability of delay that packets experience due to queuing and traffic conditions in the network. PDV is a property of a network, and is typically measured with metrics known as Packet TIE, Floor Packet Population metrics, and often the delay distribution is viewed as a histogram.

There are limits and impairment profiles for PDV that are defined by ITU-T standards which are applicable to testing equipment to establish their resilience to PDV. These profiles and limits also apply to devices with emulated PDV impairment.

PTP devices such as boundary clocks and ordinary (slave) clocks derive their frequency synchronization and Time of Day directly from the PTP packet stream, which may be subject to PDV. Due to this fact, PDV can lead directly to wander in the recovered clock signal.

Wander. Wander is a physical layer deviation of a clock signal when compared with a reference. Wander is normally measured with metrics such as Time Interval Error (TIE), MTIE & TDEV. Clocks recovered from packet timing signal flows have wander resulting in large part from PDV in the packet network.

PTP devices such as boundary clocks and ordinary clocks derive their frequency synchronization and Time of Day directly from the PTP packet stream which may be subject to PDV; therefore, PDV can lead to wander...

Limits for wander recovered on PTP ordinary clocks are defined by a number of ITU-T standards.

Principles of OnPath Support. Networking equipment such as switches and routers may be equipped with PTP features known as on-path support, that enable them to reduce the negative effects of PDV on a synchronization network. There are two elements of synchronization which are affected by PDV and delay in the synchronization network, time accuracy and frequency accuracy.

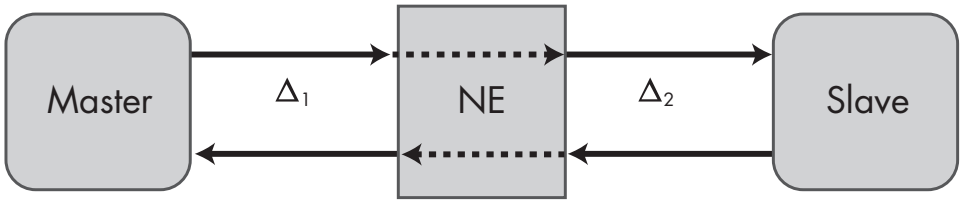
In Synchronization Networks, time transfer accuracy is bounded by transit delay asymmetry (1 and 2), as illustrated below. Delay asymmetry may be caused by dynamic delay differences (queuing, congestion) between transmit and receive paths, alternate paths for transmit and receive, rate-adaptation in the network element, or other factors. PTP assumes the path is symmetric in order to compute the time offset at the slave end.

That is, time synchronization utilizes the delay-request/delay-response mechanism together with sync-messages to calculate one-way delay as one-half the round-trip transit time. If the delay path is not symmetric, then an error in the time synchronization occurs.

Frequency transfer accuracy is impaired by transit delay variation, or PDV. The PTP slave device uses the interval of time between timestamps in PTP sync or follow-up packets to derive frequency synchronization. If this interval of time is not constant, or if it has any variability due to variation in delay, then frequency accuracy suffers.

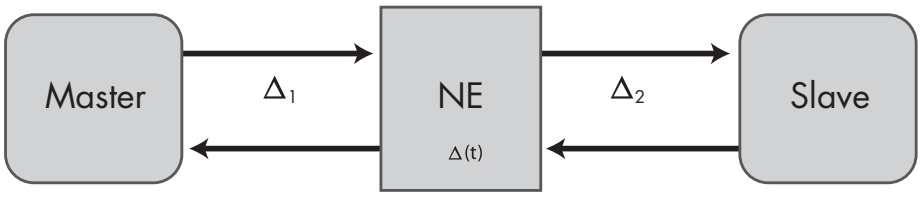
On-path support attempts to improve both frequency and time synchronization by minimizing or eliminating transit delay asymmetry in the NE, and minimizing or eliminating transit delay variation (PDV) in the NE.

PTP - aware Network Element

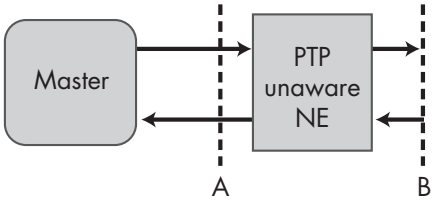


$\Delta\,(t) \approx$

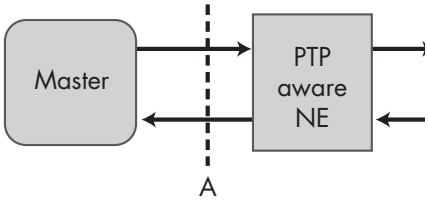
PTP - unaware Network Element



Consider a hypothetical slave deployed just before or just after the NE.



Slave at A ≠ Slave at B



Slave at A ≈ Slave at B

Without on-path support the slave at B has different time/wander behavior compared to the slave at A. Performance is dependent on the load of the NE. With on-path support the slave at B has (ideally) the same time/wander behavior compared to the slave at A. Performance should be independent of the load of the NE.

There are two forms of on-path support considered in PTP (IEEE-1588):

Boundary clock. A boundary clock "regenerates" the timing flow. That is, a boundary clock appears as a slave to the upstream master and synchronizes its time-clock to that master. The boundary clock appears as a master to downstream slaves and thereby transfers its time-clock downstream. Note that a boundary clock cannot mitigate the time error introduced by the asymmetry in the transmission medium either upstream or downstream.

Transparent clock. A transparent clock acts "invisible" by providing a timestamp correction term. There are two forms of transparent clocks. The end-to-end transparent clock provides a correction that reflects the dwell-time of the packet within the equipment itself. A peer-to-peer transparent clock includes in the correction its own internal delay as well as an estimate of the round-trip delay between itself and its upstream device. Neither type of transparent clock can mitigate the time error resulting from asymmetry in the transmission medium.

Testing Boundary Clocks

Boundary clocks are being built and deployed today and there is an immediate need for testing. Experience has indicated that testing during the development phase can be extremely useful in identifying equipment design issues.

Boundary clocks are PTP devices that may be positioned at a network boundary such as subnet boundary, provider edge or anywhere that a router would typically be employed. A boundary clock (BC) has one slave port, which is connected to a Grand Master clock through the network, and it derives its frequency and time synchronization from this slave port.

The boundary clock also has one or more master ports that are connected to slaves downstream. Sync and Follow-up packets are received on the slave port, and then the boundary clock creates new Sync and Follow-up packets that are sent to the slave devices connected to its master ports. The time stamps included in these outgoing packets are generated by the BC using its PTP implementation.

There is a potential for timestamp error, or time error, due to many factors, including queuing delays, inaccurate clock recovery on the slave port, network conditions between the grand master clock and the boundary clock (such as devices without on-path support), variables in implementation or performance of the PTP process or algorithm, etc. There also may be packet-layer errors such as queuing delay and head-of-line blocking, QoS effects, etc. that can compound any errors in the timestamps in these packets.

The difference between the timestamp time and actual time of a PTP sync or follow-up packet is the time error; the difference between the actual time of a PTP packet and what it should be is the PDV. While PDV traditionally applies to delays that packets encounter as they traverse many hops through a network, due to the complexities of a boundary clock, sync packets emerging from the BC may have non-linear timing errors that cannot be distinguished from PDV and have the same effect on the clock recovery of the slave downstream as traffic-induced PDV.

New standards are emerging such as ITU-T G.8273 that may help evaluate the synchronization quality of boundary clocks. Annex A and Annex B of G.8273 represent the first clear consensus in the industry regarding testing boundary clocks.

Regardless, boundary clocks are being built and deployed today, and there is an immediate need for testing. Experience has indicated that testing in the development phase can be extremely useful in identifying equipment design issues.

Testing Challenges

In most conventional methods boundary clocks are tested as a neighbor to a slave clock and the test result derived from the slave's output. These methods do not directly evaluate the performance of the boundary clock, and in fact the results are necessarily decoupled from the boundary clock and are often more an indication of the slave clock performance.

The implementation of boundary clocks by manufacturers varies, and as a result not all boundary clocks have common interfaces or topologies. For example, some boundary clocks lack recovered frequency interfaces or 1PPS phase that are externally accessible. This can add complexity to testing requirements.

Given that there is a potential source of time error impairment (static and dynamic) caused by a boundary clock, their performance must be evaluated. The impact of a boundary clock on frequency recovery may be comparable to that of an ordinary switch with no on-path support. Methods of testing that consider both static and dynamic impairments are required for validating time/phase transfer.

Traditional testing with frequency metrics and PDV impairment testing are necessary, but not sufficient, for boundary clocks, and measurement of time error of the PTP packets is becoming increasingly important. Frequency-impairment metrics such as MTIE and TDEV serve to quantify stability, namely the strength of the dynamic portion of the time error; estimating the constant time error provides an indication of the nominal accuracy of the time transfer. Methods for accurately identifying and analyzing the timing impairments introduced by a boundary clock are maturing.

Given that there is a potential source of time error impairment caused by a boundary clock, their performance must be evaluated. Methods that consider both static and dynamic impairments are required.

Testing Time & Frequency Synchronization on Boundary Clocks

ITU-T G.8273 considers direct evaluation of boundary clocks. An arrangement for testing on-path support is described in ITU-T G.8273 Annex B.

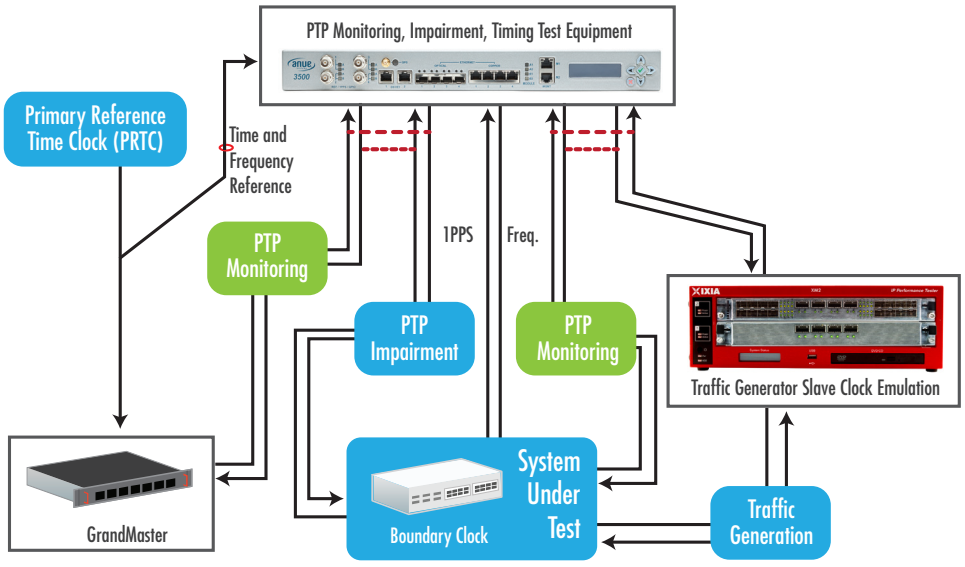


Figure 2 – On-Path Support Testing Arrangement – Boundary Clocks

Test Steps

1. Connect the equipment as shown in the diagram

   a. Ixia Anue 3500 for PTP monitoring and impairment connected in-line between the Grand Master clock and the Boundary Clock DUT Ethernet path

   b. Ixia Anue 3500 for PTP monitoring in-line between the Boundary Clock DUT and the slave or emulated slave

   c. IxNetwork Traffic Generator connected to the Boundary Clock DUT Ethernet interfaces

   d. Ixia Anue 3500 and Grand Master Clock connected to a common Time/Frequency reference

   e. Connect recovered 1PPS and frequency signals from the Boundary Clock DUT, if available

2. Add PDV impairment using the Ixia Anue 3500 between the Grand Master and the Boundary Clock DUT. Impairment may be G.8261 test cases, impairment captured from a live network, or custom impairment profile
3. Add background traffic from the IxNetwork to pass through the Boundary Clock DUT
4. Monitor/measure the PDV and 1588 Time Error on the Grand Master side and the Slave side of the Boundary Clock DUT. Verify that the Slave side Time Error meets the desired limit (e.g. 1.5us) using the Ixia Anue 3500
5. Measure the Time Error of the 1PPS and MTIE/TDEV of the recovered Frequency from the Boundary Clock DUT using the Ixia Anue 3500. Verify that the 1PPS Time Error meets the desired limit (e.g. 1.5us) and the frequency meets the desired standard (e.g. G.824 Sync masks for MTIE & TDEV).

It is important to consider the cumulative effect of a chain of transparent clocks connected in a network, where the PDV and also any error or inaccuracy in the correction field is accumulated.

Testing Transparent Clocks

Transparent clocks are PTP devices that operate as normal switches, but they update the correction field of the PTP packets with a value equal to their residence time, or the time the packet was delayed in the switch. The next device in the network can then account for the PDV that is introduced by the transparent clock by adjusting the time-stamp value using the correction field.

It is assumed that the transparent clock is going to introduce PDV in the same fashion as a normal switch: depending on traffic and load conditions, the delay each packet experiences may vary. The purpose of the transparent clock function using on-path support is to remove the effect of this PDV by informing downstream devices of precisely what these delays were on a packet-by-packet basis. It is important to consider the cumulative effect of a chain of transparent clocks connected in a network, where the PDV is accumulated and also any error or inaccuracy in the correction field is accumulated.

The effectiveness of the reduction in PDV that is accomplished by the on-path support of the transparent clock depends on the accuracy of the correction field value relative to the actual residence time of the packet. Many factors influence this accuracy, including the accuracy of the frequency and timestamp accuracy in the transparent clock's PHY. Variations in implementation of the transparent clock feature may also heavily influence the accuracy of the correction field values. More importantly, background traffic in the transparent clock, or PDV impairment in the PTP traffic stream before it reaches the transparent clock, along with non-zero values in the correction field of these packets, may introduce errors that are difficult or impossible to anticipate without testing directly.

New standards are emerging, such as ITU-T G.8273, that may help evaluate the accuracy of transparent clocks. Until such standards are fully adopted, there remains a need to test transparent clocks that are being developed and deployed today since testing in the development phase can be extremely useful in identifying equipment design issues.

Testing Challenges

Traditional PTP or IEEE1588 testing of transparent clocks focused primarily on their effect on the accuracy of a downstream device, such as a slave clock. These methods fail to test the transparent clock directly, and also do not provide a uniform or repeatable method of comparing one device to another or assess the effectiveness of changes in the product during the development phase. In fact, traditional methods of testing transparent clocks may often depend more on the slave clock performance than on the accuracy of the transparent clock.

Considering that transparent clocks may not employ a PTP slave function, there may often be no measurable 1PPS or frequency interface available. Therefore, the accuracy of the device must be established by analysis of the correction field accuracy.

Testing Correction Field Accuracy on Transparent Clocks

ITU-T G.8273 opens the door for evaluation of the accuracy of the correction field of transparent clocks, but at this time a limit of error is not defined. An arrangement for testing on-path support which can be used for testing transparent clocks is described in ITU-T G.8273 Annex B.

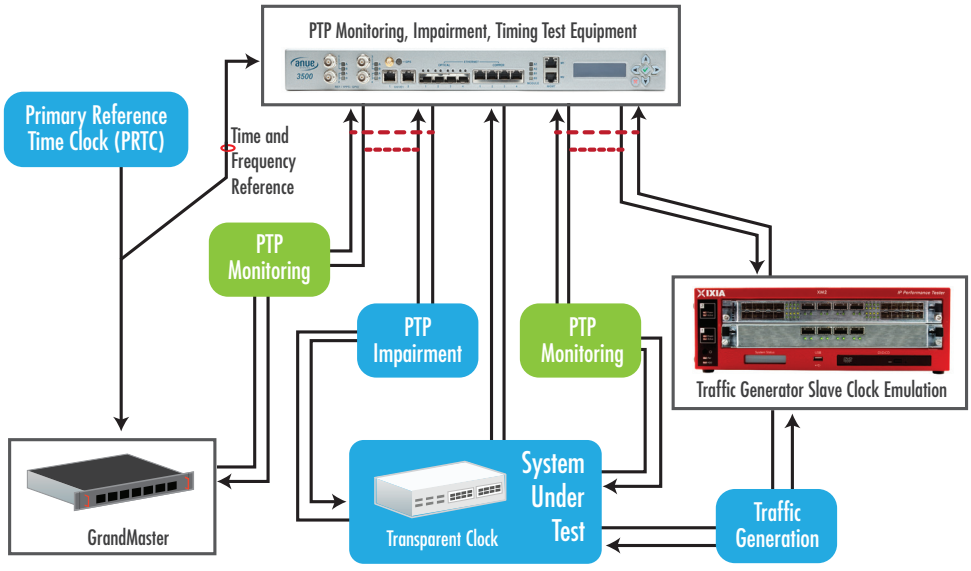


Figure 3 – On-Path Support Testing Arrangement – Transparent Clocks

In this testing arrangement, the System Under Test (TC) is situated between the Grand Master clock and a Slave Clock or emulated slave clock(s), as it would be in a production network. Test Equipment is provided for monitoring the PTP packet stream before and

New standards are emerging, such as ITU-T G.8273, that may help evaulate the accuracy of transparent clocks. Until such standards are fully adopted, the need remains to test those being developed and deployed today.

after the System Under Test (TC) in order to measure accuracy of the Correction Field and PDV introduced by the System Under Test (TC). A traffic generator is also provided in order to introduce background traffic into the System Under Test (TC) so that the PDV and accuracy can be tested under traffic load conditions.

Test Setup

1. Connect the equipment as shown in the diagram.

   a. Ixia Anue 3500 for PTP monitoring and impairment connected in-line between the Grand Master clock and the Transparent Clock DUT Ethernet path

   b. Ixia Anue 3500 for PTP monitoring in-line between the Transparent Clock DUT and the slave or emulated slave

   c. IxNetwork Traffic Generator connected to the Transparent Clock DUT Ethernet interfaces

   d. Ixia Anue 3500 and Grand Master Clock connected to a common Time/Frequency reference

2. Measure the PDV / 1588 Time Error of the PTP packet stream on both ingress and egress sides of the Transparent Clock using the Ixia Anue 3500 (no impairment applied).

   a. With PTP traffic running through the Transparent Clock DUT between the Grand Master and Slave, evaluate the PDV & Time Error of the packets on the Grand Master side of the connection and at the slave side simultaneously. Do not check the "Use Correction Field if Available" box on the Ixia Anue 3500. The difference observed in PDV & Time Error on the slave side of the DUT vs. the Grand Master side indicates the PDV introduced by the Transparent Clock DUT.

   b. Run the test in step 2a again but with the "Use Correction Field if Available" box checked. The Ixia Anue 3500 will adjust using the actual correction field values, and the resultant Slave side PDV graph, when compared with the Grand Master side graph, indicates the accuracy of the correction field.

   c. Note the absolute Time Error (error of time of day), and ensure it meets the desired requirement.

3. Add PDV impairment using the Ixia Anue 3500 between the Grand Master and the Transparent Clock DUT. Impairment may be G.8261 test cases, impairment captured from a live network, or custom impairment profile. Repeat the measurements in step 2 with PDV impairment present.
4. Add background traffic from the IxNetwork to pass through the Boundary Clock DUT. Repeat the measurements in step 2 with background traffic present.

Test Equipment Requirements

ITU-T Recommendation G.8271 considers different classes for time error accuracy. For example, Class 4 corresponds to time accuracy of between 1s and 1.5s and is representative of the accuracy required in emerging wireless networks. This accuracy is expected when timing information is delivered over a Hypothetical Reference Model network comprising up to 20 nodes with full on-path support.

That is, there will be boundary clocks in every node. Allocating one-half the accuracy budget to the unavoidable asymmetry of the transmission links, and 100ns to the Primary Reference Time Source (PRTC), the time error generation limit for each on-path support device is between 22ns and 35ns.

Testing a device to ascertain its noise generation properties of its on-path support mechanism can be achieved in two ways. In the first case the device is placed between a master clock and a slave clock and the master and slave are both referenced to the same time source so that the slave device can operate as a passive PTP probe and the effective time output of the unit under test compared to the reference.

In the second case a PTP Monitor is used to observe and time-stamp traffic between the device under test and an upstream master clock as well as the traffic between the device and a downstream slave. The time noise generation in the device is then estimated from the two time error sequences.

In both cases the measurement uncertainty is closely linked with the time error introduced by the measurement set-up itself. As with all packet-based timing measurement methods, a principal component of the measurement error is related to the time-stamping accuracy. In order to measure the noise generated by the device and compare it against 22ns, it is clear that the time-stamping accuracy in the testing devices must be substantially better, typically by an order of magnitude.

That is, in order to test boundary clocks and transparent clocks against noise generation limits, the test equipment must have time-stamping accuracy that is of the order of 2ns or better. This requires an effective time-stamping clock rate in excess of 500MHz.

The Ixia /Anue 3500 time-stamping clock rate is effectively 625MHz.

In the first case the measurement includes any time error in the synchronization of master and slave through the common reference time source. As well as any time error generated by the master and slave devices themselves. It is important that this net time error be constrained to approximately one order of magnitude less than the quantity being measured. To verify on-path support efficacy, this net time error must be of the order of 2ns or better.

In the second case, the PTP monitor can use the same clock for time-stamping both sides of the device under test provided that the PTP monitor equipment has multiple ports in the same machine. The system clock time error is thus a “common mode” phenomenon and it suffices that the equipment clock be stable.

The Ixia Anue 3500 provides multiple ports and has an internal system clock stability that corresponds to the order of picoseconds over the duration of the measurement.

Upon quickly completing hundreds of tests, a leading manufacturer was able to confidently harden and optimize a new design, contract suppliers, and move forward with the planned launch of a new mobile device.

Element	Requirement
Time Error for each on-path support device allowable	22-35 ns
Time stamping accuracy required for test equipment	2 ns or better
Ixia Anue 3500 Time stamp accuracy	1.6 ns
Ixia Anue 3500 Clock Stability	picoseconds

Conclusion

Migration from legacy mobile backhaul network synchronous transports to Ethernet poses distinct challenges that require vigorous testing and validation. Ixia is helping to build the test products and the information base that engineers need to develop and execute plans for testing functionality, timing accuracy, performance, and scalability required to implement these changes. We are a leader in the timing and synchronization space, actively participating in, and one of the main contributors to, ITU-T SG15Q13 activities, as well as participating in WSTS, ITSF, ISPCS, and other industry events.

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